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A Micro-Power CMOS RF Front-end for Embedded Wireless Devices

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Outline

- **Introduction to Wireless Integrated Network Sensors (WINS) Project:** Network, Applications, Nodes
- **Unique Front-end Requirements**
- **RF Architecture:** Preselector, LNA and Mixer Architecture
- **Future work:** (WINS integration)
- **Summary**

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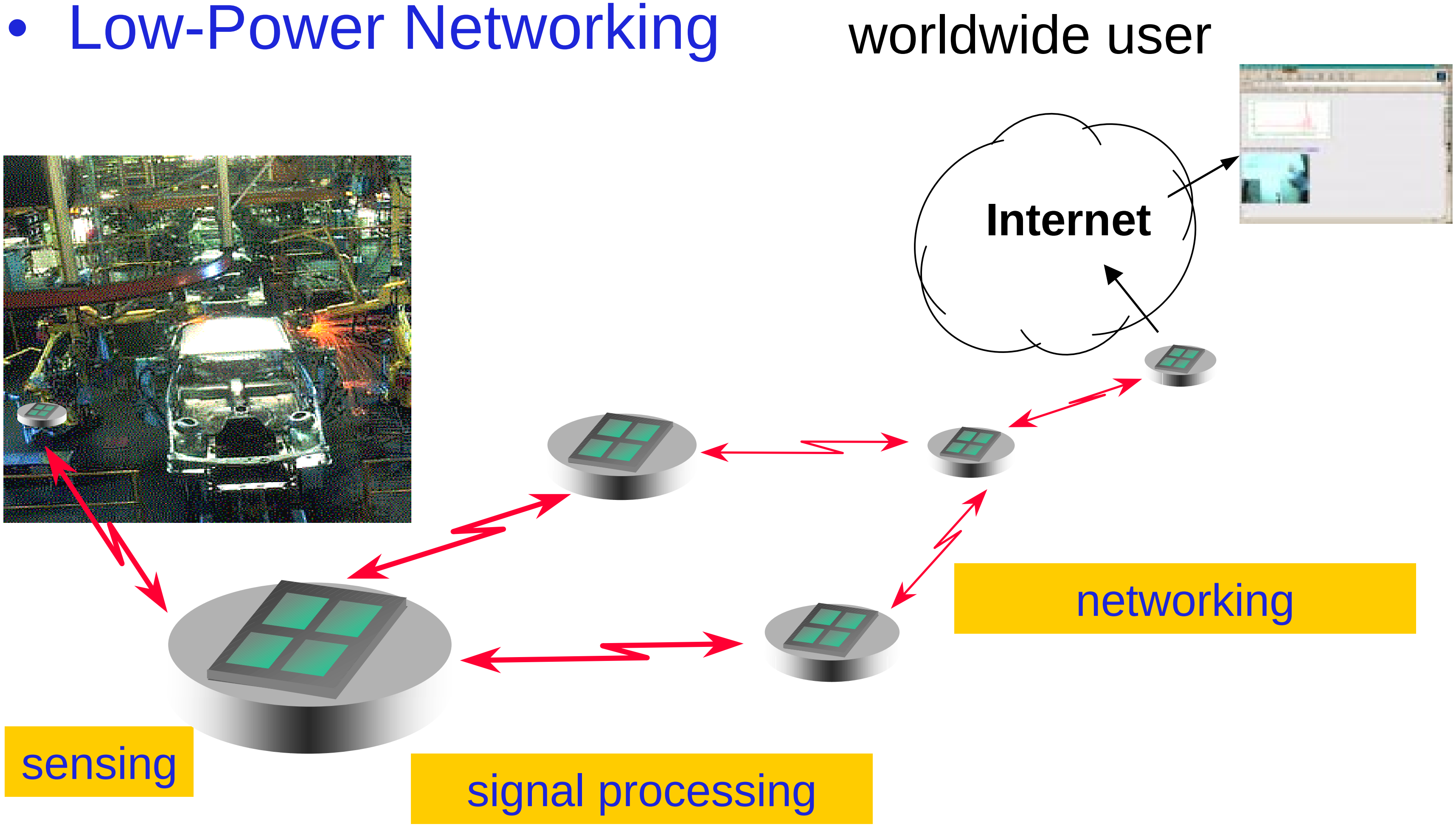
(Wireless Integrated Network Sensors) WINS

- Low-Power Networking



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WINS Applications

Consumer

Defense security

Transportation systems

Medical instrument internetworking

Industrial controls

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Network Characteristics

- Dense node distribution
- Short range (< 30m)
- Low bit rate (< 100kbps)
  (Typical sensor systems are band limited)
- Latency tolerant
- Compact cell
- 3 year life
- 100 μW average
- 3 mW peak

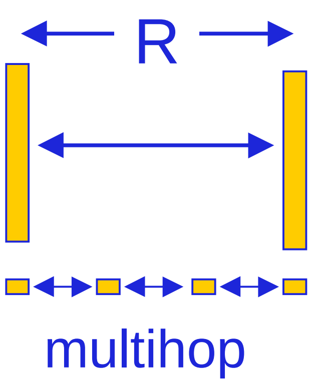
Implement multihop for power:

RF path loss:

$$P_{rec} \propto 1/R^{\alpha} \; (\alpha \approx 3 - 5)$$

Relative system power advantage for N-hop chain:

$$P_{tot}(N)/P_{tot}(1) \;\propto\; 1/N^{(\alpha-1)}$$



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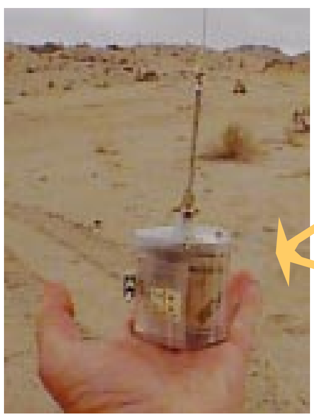
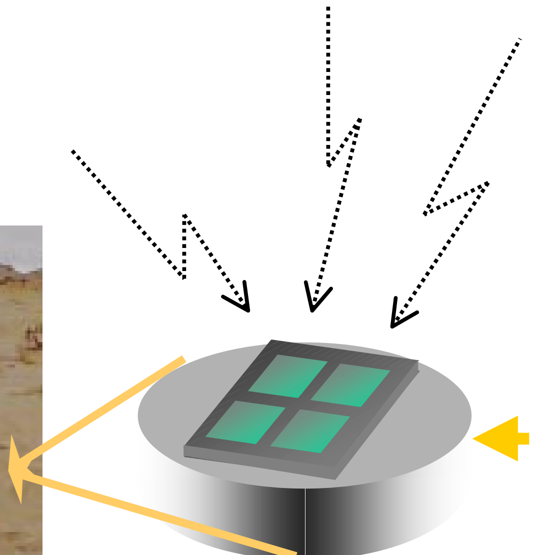
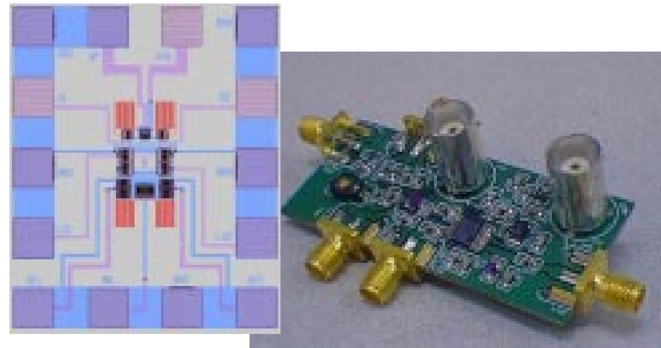
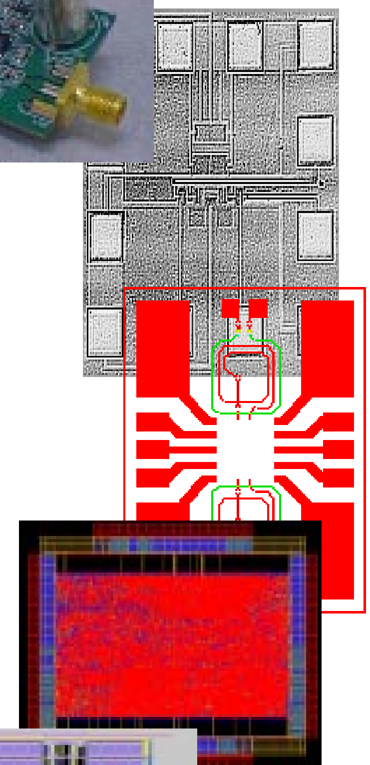
WINS Nodes

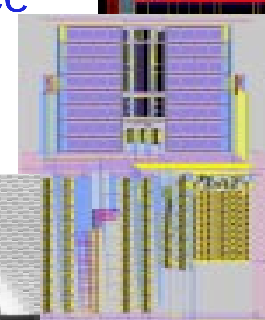








- WINS RF Modem
- Network Interface
- Memory
- Microcontroller
- State Machine
- DSP
- ADC
- Sensor Interface
- Sensors



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WINS vs. Existing wireless system

Characteristic	Wireless LAN	Cellular Telephony	WINS
Range	~ 200m	~ 5km	≤ 30m
Data Throughput	~ 2-10Mbps	~ 10kbps	≤ 100kbps

- Conclusions:
- **Range and bandwidth reduction : *60 - 80dB gain in link budget***

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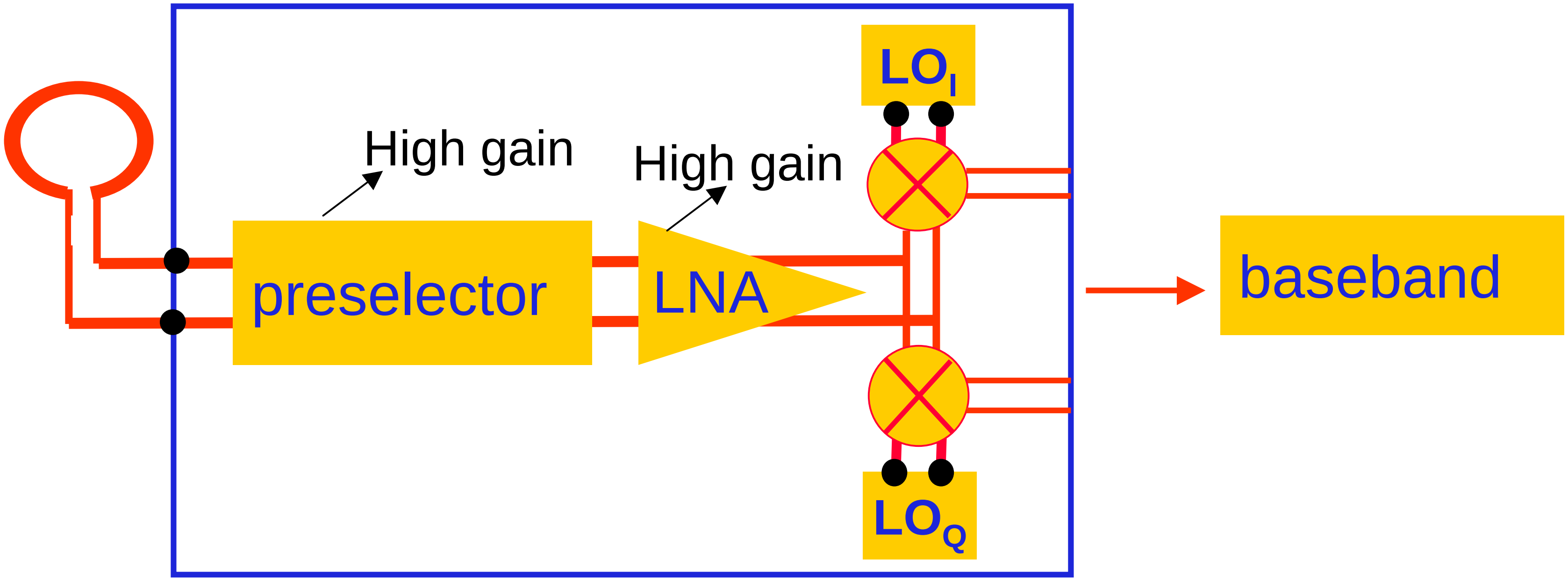
Why Design a New Receiver?

- **Performance Specifications of receivers:**

	Cellular	Bluetooth	WINS
Noise Figure	**8dB**	**Est (- 26)**	**~ 25dB**
Sensitivity	**-102dBm**	**-70dBm**	**~ -70dBm**
Data rate	**~10 kbps**	**1Mbps**	**≤ 100kbps**
Current consumption	**35 - 40mA**	**≤ 20mA**	**~ 1 mA**

- Challenge: Minimum noise figure and best sensitivity for long range communications.
- **Specifications of the front-end receiver for WINS project:**
  - Digital CMOS transistor
  - Current consumption ≤ 200 µA
  - Gain ≅ 20 - 25dB
  - Noise figure ≅ 20 dB
- Challenge: Micro power for short range communications (30 m)

Receiver Architecture



Goal: 1mA entire receiver system peak current drain

- High-Q inductive loads
- Off chip integration: LTCC components

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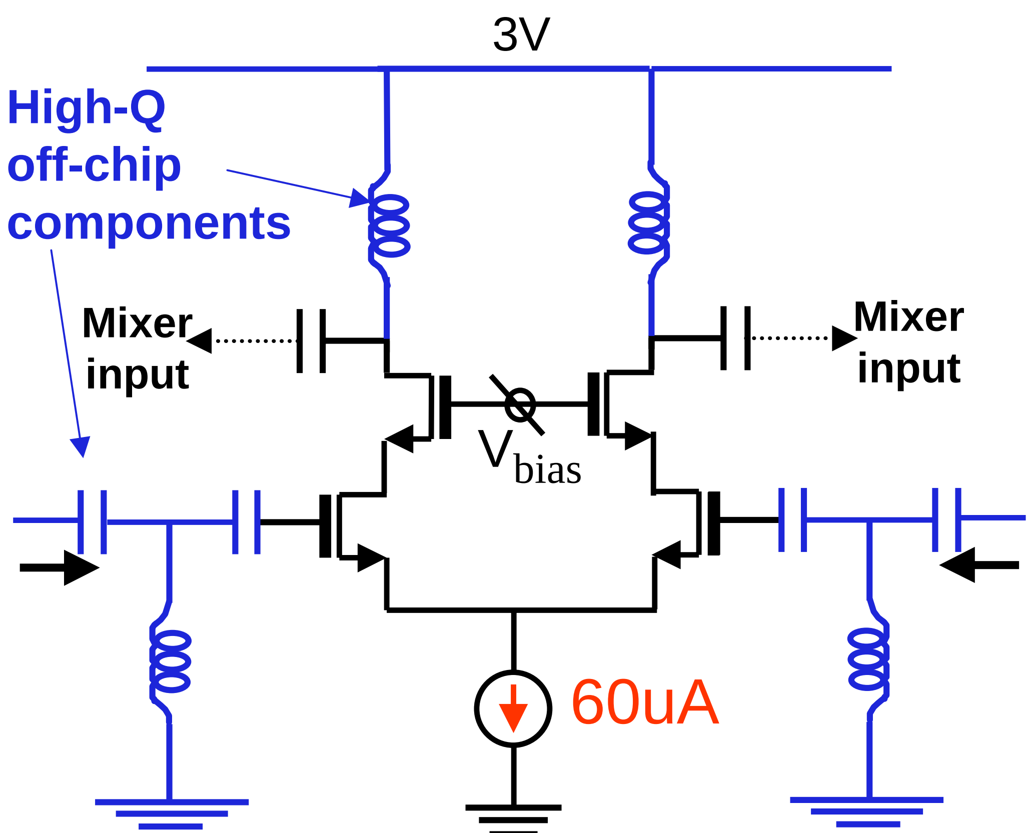
Differential Preselector/LNA



Gain achieved by:

- **Preselector:** High Q elements
- **LNA transistors g_m:** Small due to the small current and relatively small transistor sizes
- **LNA output Impedance:** High Q components to generate large impedance at the output
- **Mixer input:** High impedance

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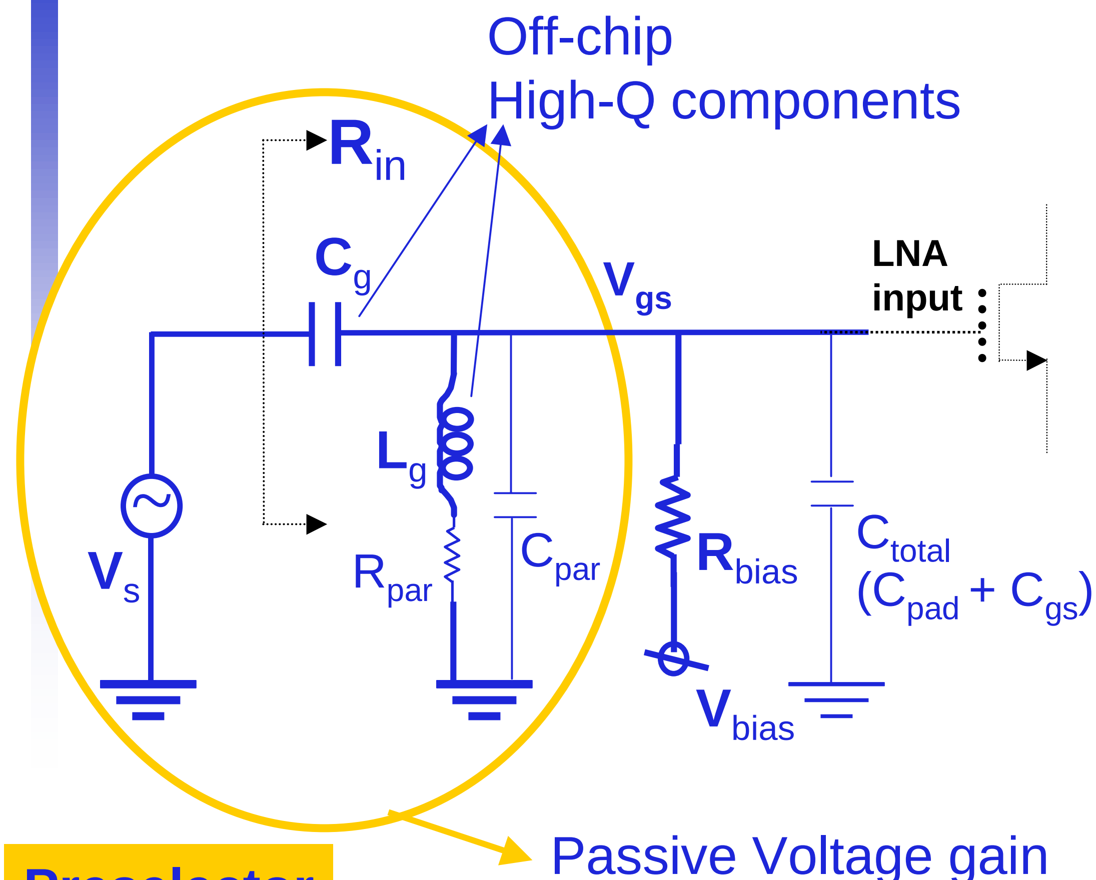
Preselector



Preselector

- **Filtering**
- **Matching**

Choose L and C:

$$\omega_{res} = R / \sqrt{L((C_g + C_{total})R^2 - L)}$$

$$R \rightarrow \infty \quad \omega_{res} \approx 1/\sqrt{L(C_g + C_{total})}$$

Input impedance at ω_{res} :

$$R_{in} \approx L/R_{bias}(C_g \| C_{total})$$

- **Gain from V_s to V_{gs}:**

$$V_{gs}/V_s \approx R\sqrt{(C_g \| C_{total})/L}$$

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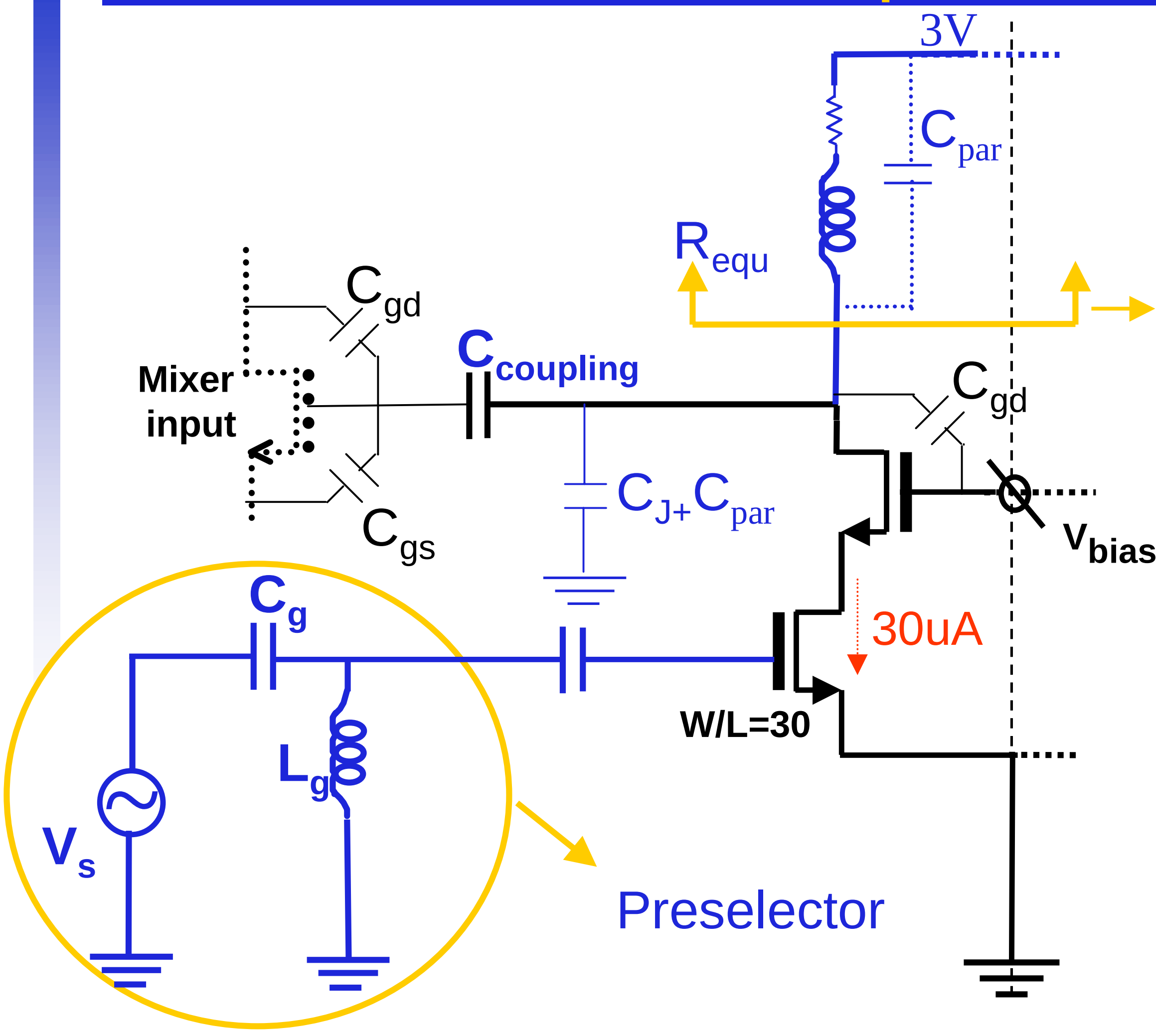
Half Circuit of the Preselector/LNA Including Off-chip Elements



- **LNA output impedance at ω_{res} :**

  $R_{equ} = L / RC_{total}$

- **Total gain:**

  $A_v = g_m R_{equ} A_{preselector}$

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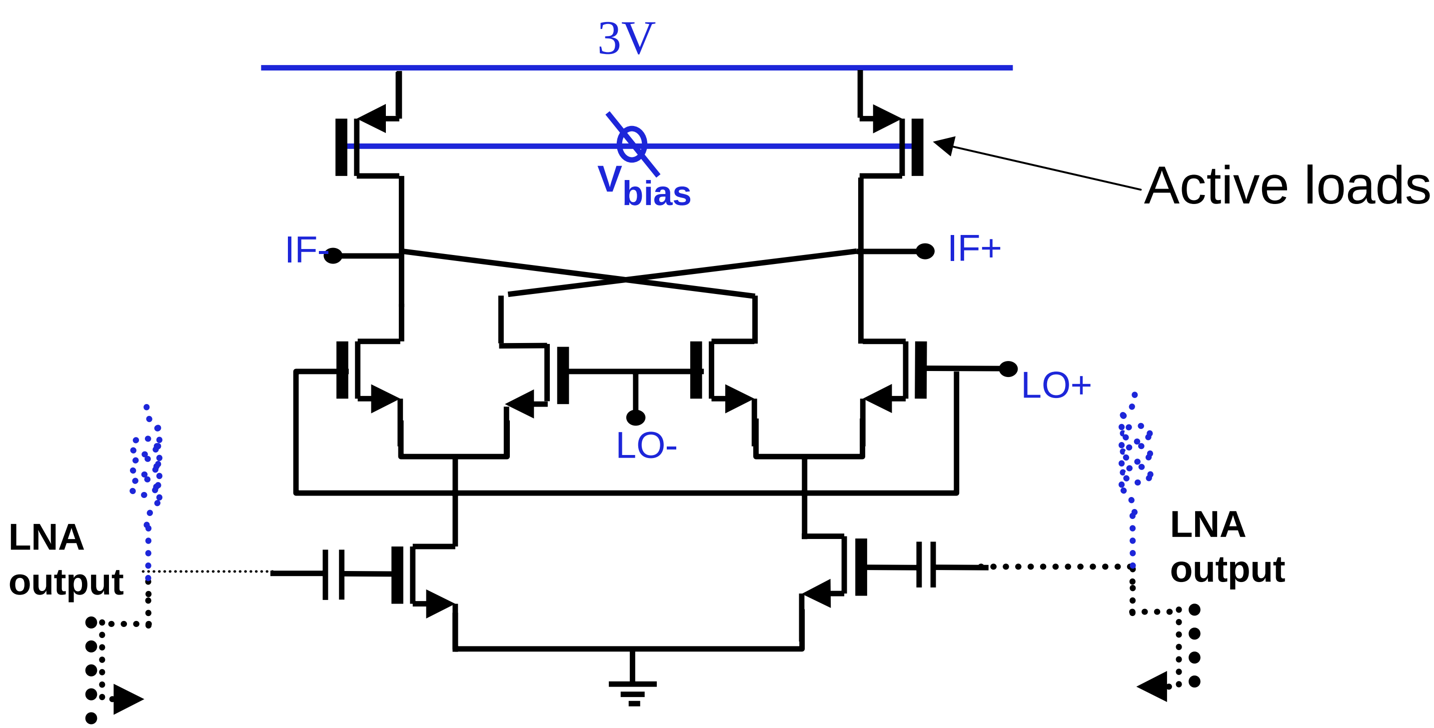
Mixer

- Weak inversion
- Double-balanced Gilbert Cell
- Direct conversion
- 50 µA core supply current at 3V
- Output bandwidth > 100kHz
- High output impedance



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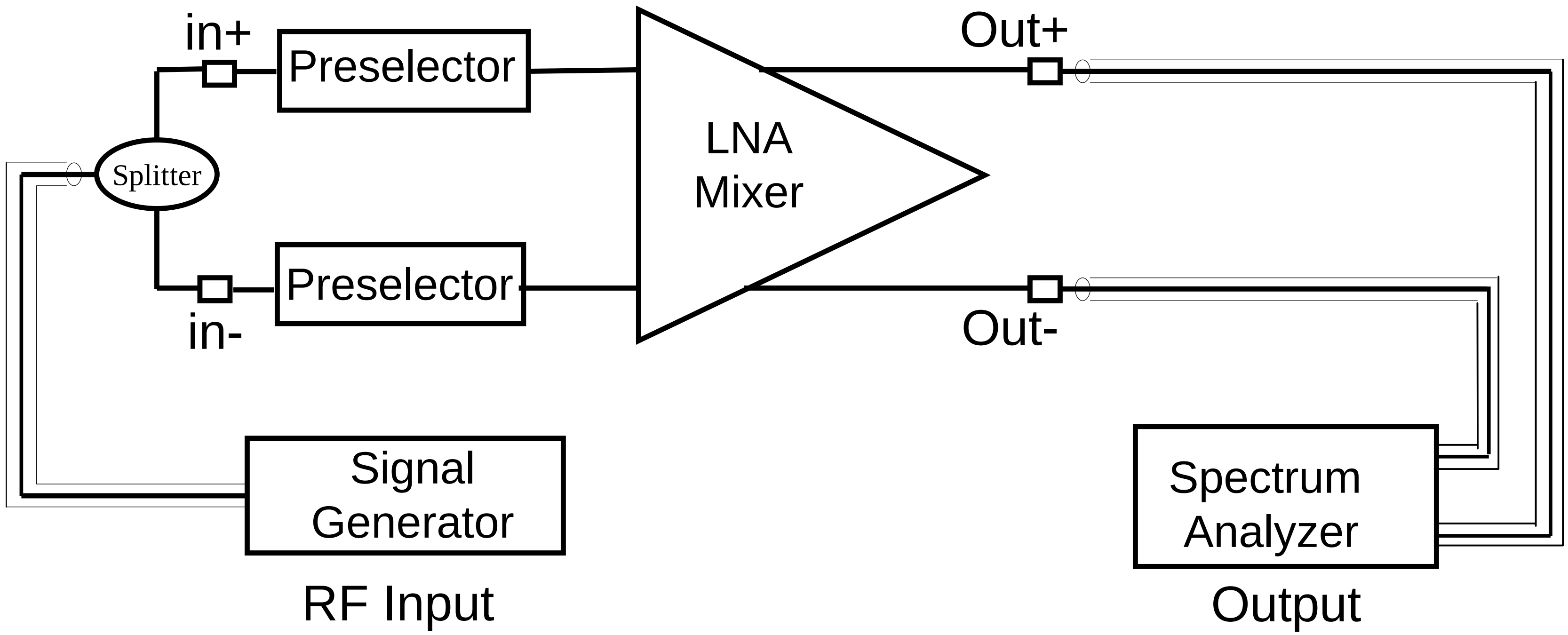
Test Setup

- Testing Preselector, LNA and Mixer:



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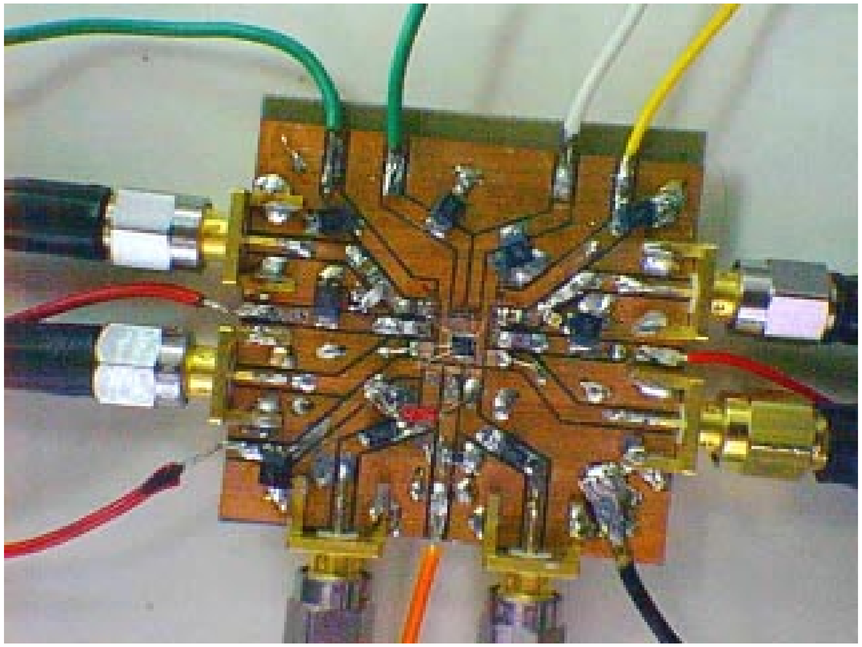
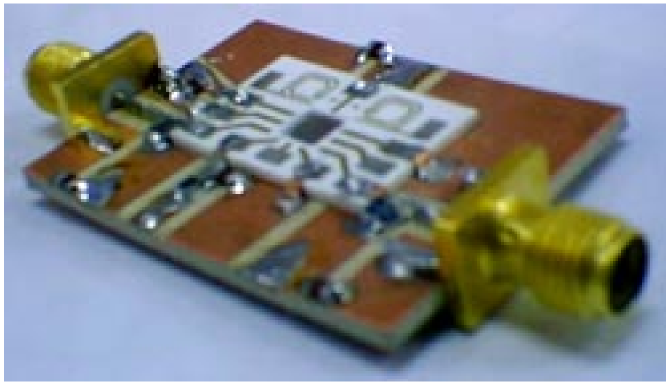
Testing



Front-end with off-chip components



VCO on LTCC substrate

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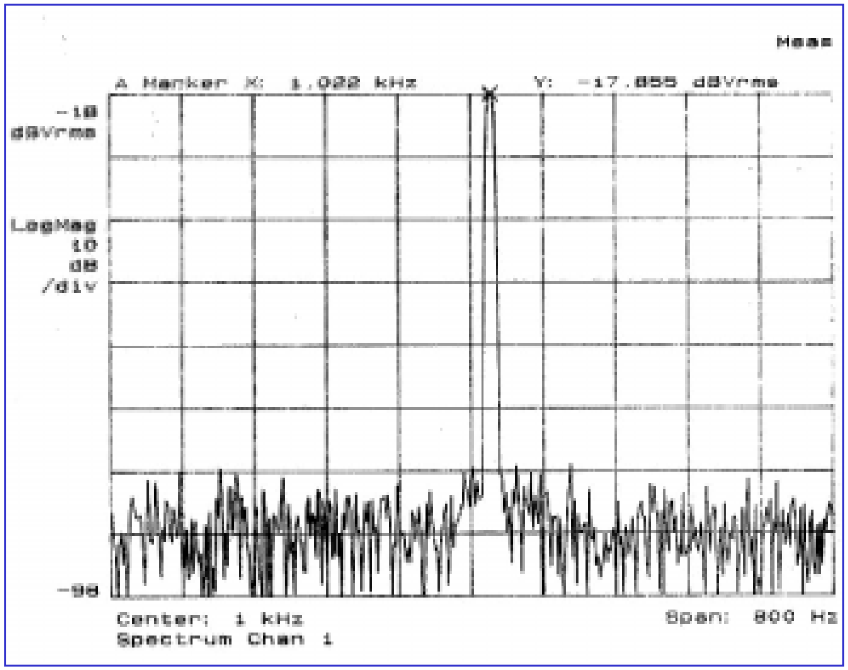
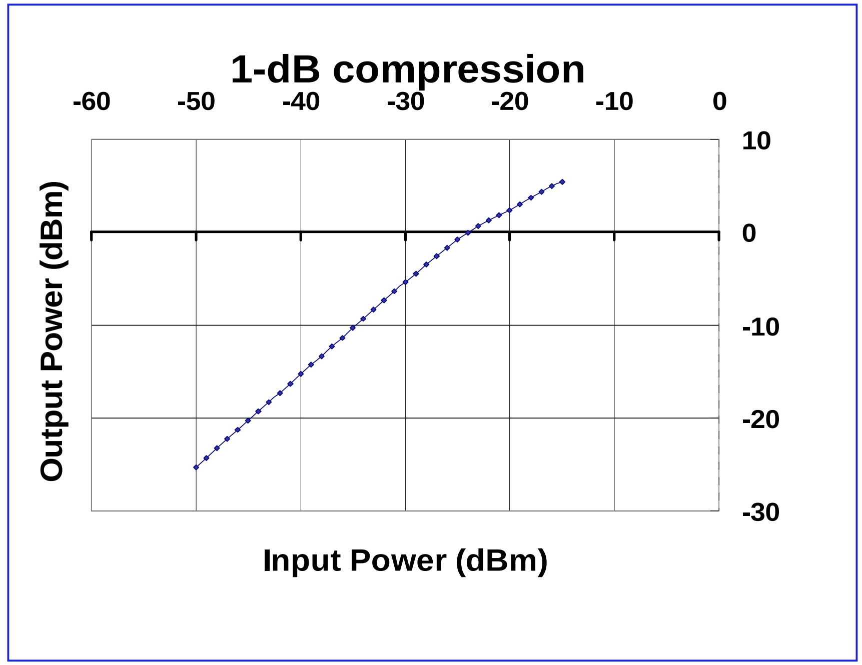
Gain Results

Gain = 25dB

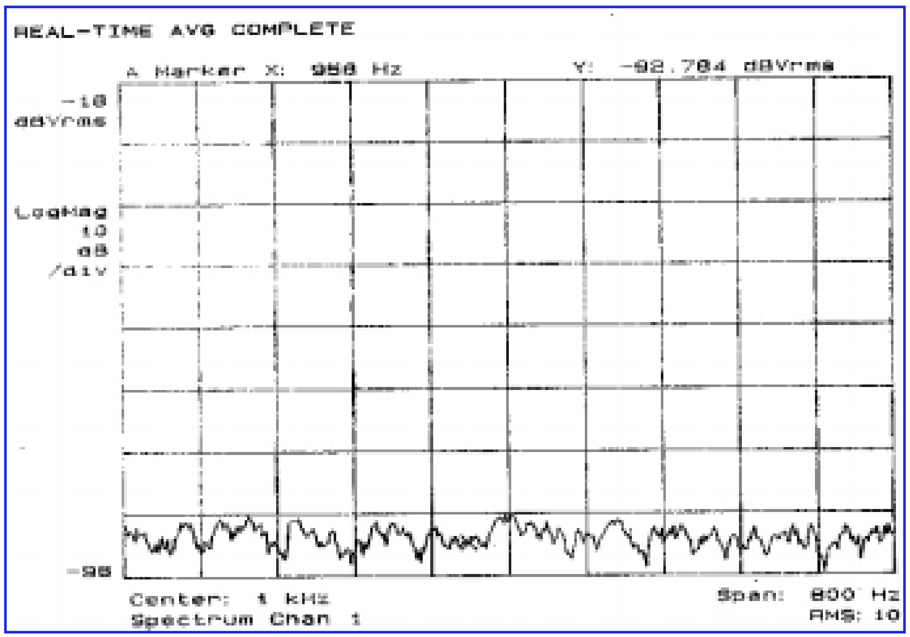


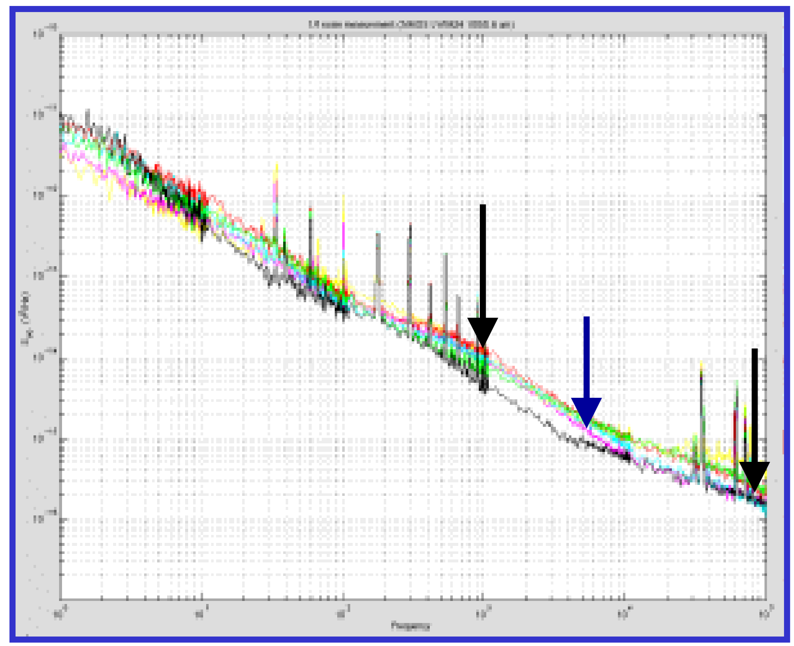


LNA input = -43dBvrms
Mixer output = -17.85dBvrms

1-dB compression at -25dBm (effective power)

Noise Measurement for Front-end





This front-end:
At 1KHz: NF ≈ 28dB
At 25KHz: NF ≈ 19.5 dB

1/f S_{VG} measurement
(NMOS 100/0.6 um)

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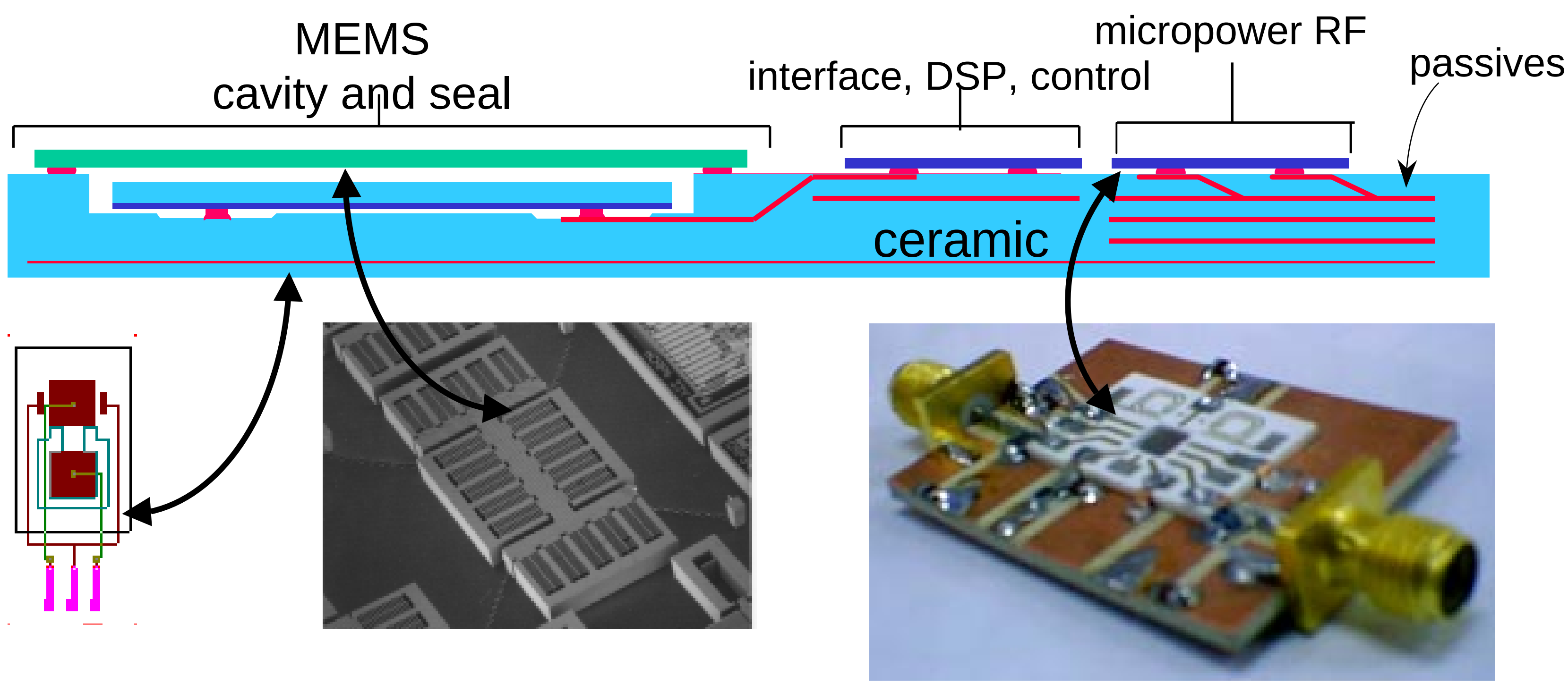
WINS Integration

- Low Temperature Co-fired Ceramic
- Scrantom Engineering

L = 20nh Q ≈ 20 @ 1GHz



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Summary

- WINS project RF components trade off sensitivity for greatly reduced power consumption
- A front-end receiver with a total current consumption of 110 μA has been developed and tested in 0.8 μm CMOS technology
- The front-end includes a preselector which provides gain and filtering before the LNA
- The receiver has: Gain = 25dB, NF = 19.5dB, 1-dB compression = -25dBm,

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