Ch 1.
Introduction to Embedded Systems

Part B
Embedded ARM Applications

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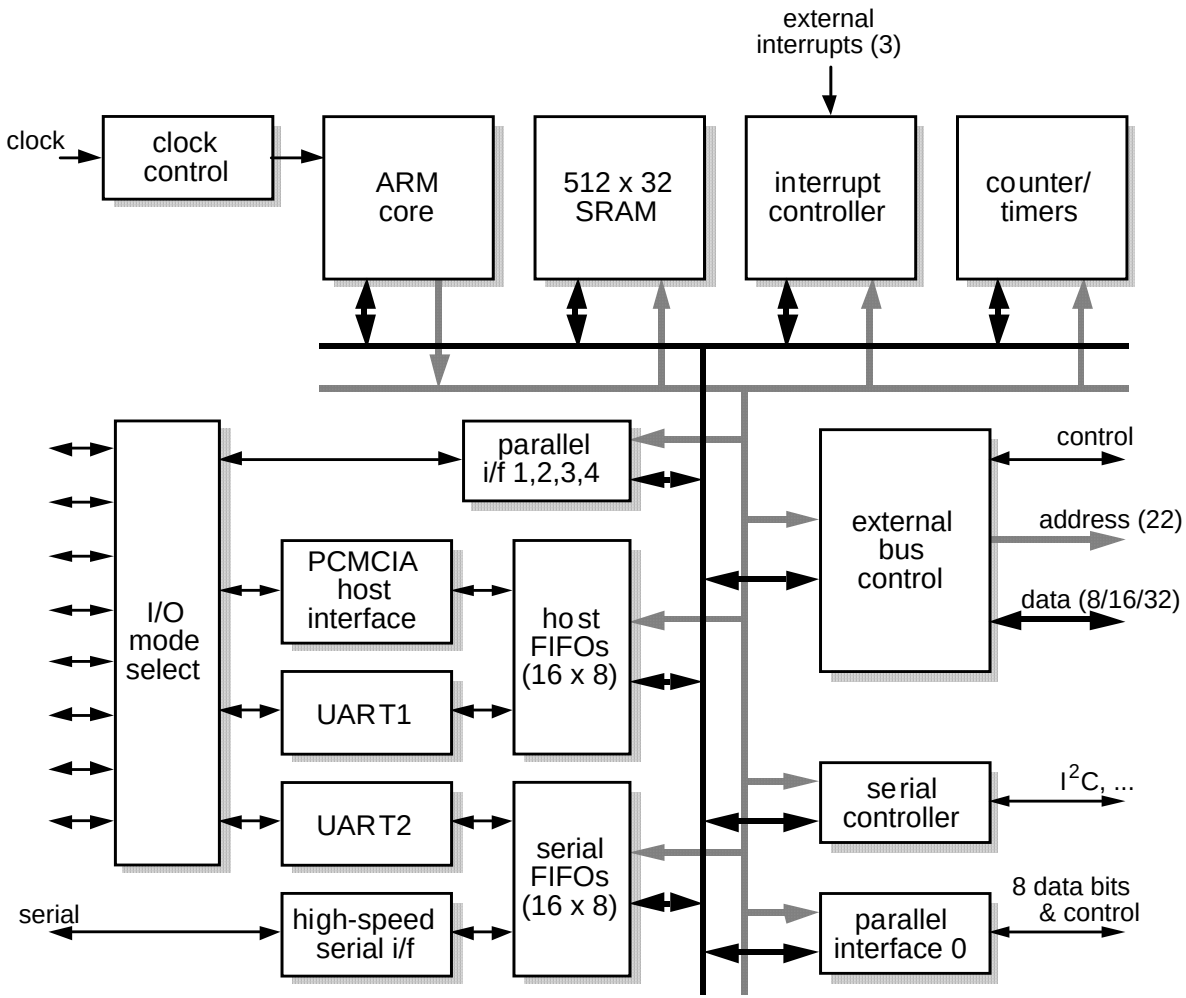
Overview

- Trends in embedded system design
  - Integrate all the major system functions apart from some memory components into a single chip
  - Benefits in terms of component costs, reliability, and power-efficiency
  - Advance in semiconductor process technology: millions of transistors built cheaply
  - The era of complex systems on a single chip
- Several examples of ARM-based 'system on chips'

1.7 The VLSI Ruby II Advanced Communication Processor

- **Ruby II advanced communication processor chip**
  - VLSI Technology, Inc
  - Organization –>



The VLSI Ruby II Advanced Communication Processor (II)

- Ruby II organization
  - Based on an ARM core
  - 2 Kbytes of fast (zero wait state) on-chip SRAM
    - Critical routines can be loaded to get the best performance and minimum power consumption
  - Peripheral modules
    - PCMCIA interface
    - Four byte-wide parallel interfaces
    - Two UARTs
    - Byte-wide FIFO buffers
    - Synchronous communications controller
    - Serial controller: I^2C for battery-backed RAM, real-time clock, E^2PROM, and audio codec
  - External bus interface
    - 8-, 16-, and 32-bit data buses and flexible wait state generation
  - Counter/timer block
    - Three 8-bit counters connected to a 24-bit prescaler
  - Interrupt controller
    - Programmable control of all on- and off-chip interrupt sources

The VLSI Ruby II Advanced Communication Processor (III)

- Ruby II power-management modes
  - 1. On-line – all circuits are clocked at full speed
  - 2. Command – the ARM core runs with 1 to 64 wait states but all other circuitry runs at full speed. An interrupt switches the system into on-line mode immediately.
  - 3. Sleep – all circuitry is stopped apart from the timers and oscillators. Particular interrupts return the system to on-line mode.
  - 4. Stopped – all circuits (including the oscillators) are stopped. Particular interrupts return the system to on-line mode.

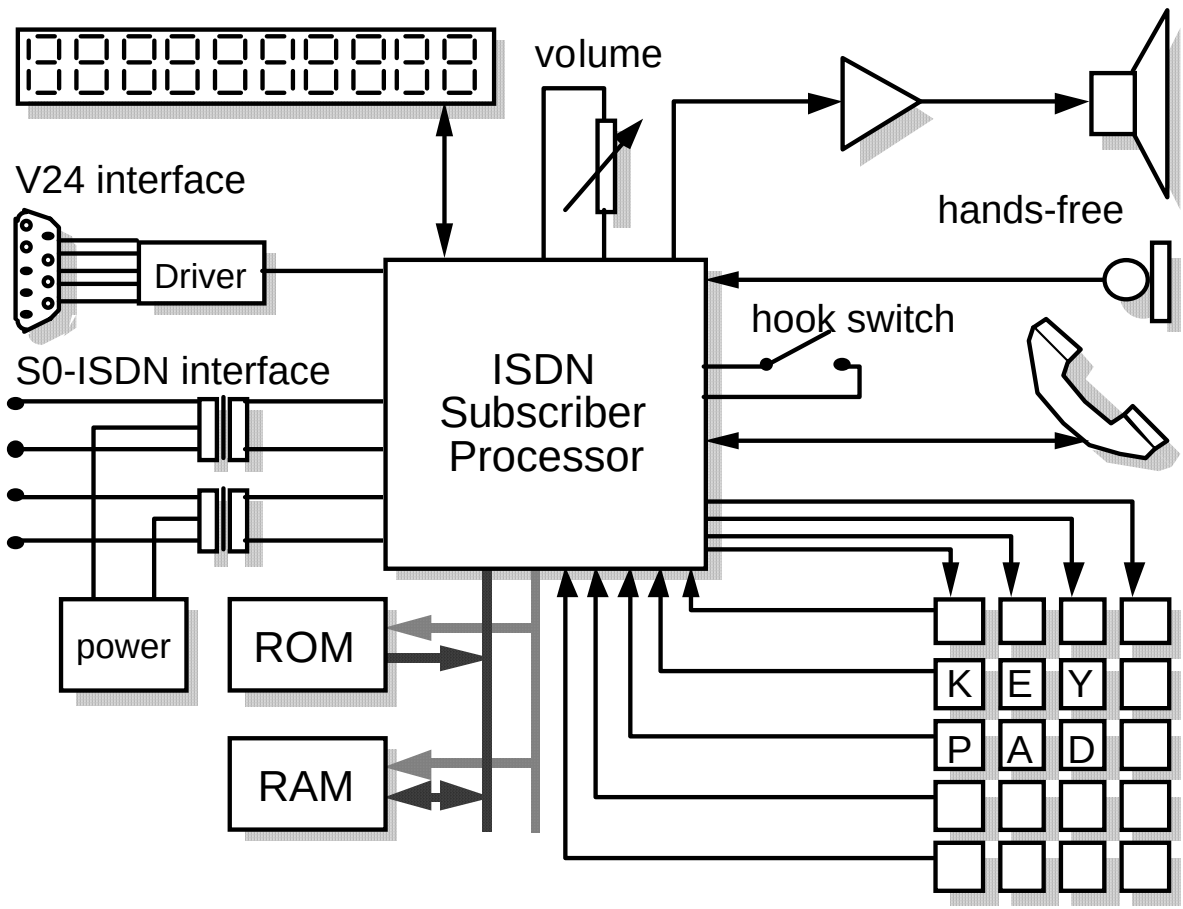
- Packaging
  - 144- and 176-pin thin quad flat packs
  - Up to 32 MHz at 5 V.
  - At 20 MHz, 30 mA in on-line mode, 7.9 mA in command mode, 1.5 mA in sleep mode, and 150 uA in stop mode.

1.8 The VLSI ISDN Subscriber Processor (VIP)

- **VIP**
  - Programmable engine for ISDN (Integrated Services Digital Network, a digital telephony standard) subscriber communications
    - Developed by Hagenuk GmbH
    - Licensed to VLSI Technology for sale as ASSP (Application Specific Standard Part)
  - Incorporates most of the circuitry required to implement a full-feature ISDN terminal, supporting voice, data, and video services
    - ISDN S0-interface, a numeric keypad, a number display, a microphone and an earphone
  - Applications
    - ISDN terminal equipment: PABX telephones, H.320 videophones, integrated PC communications
    - ISDN to DECT (Digital European Cordless Telephone) controllers
    - ISDN to PCMCIA communication cards.

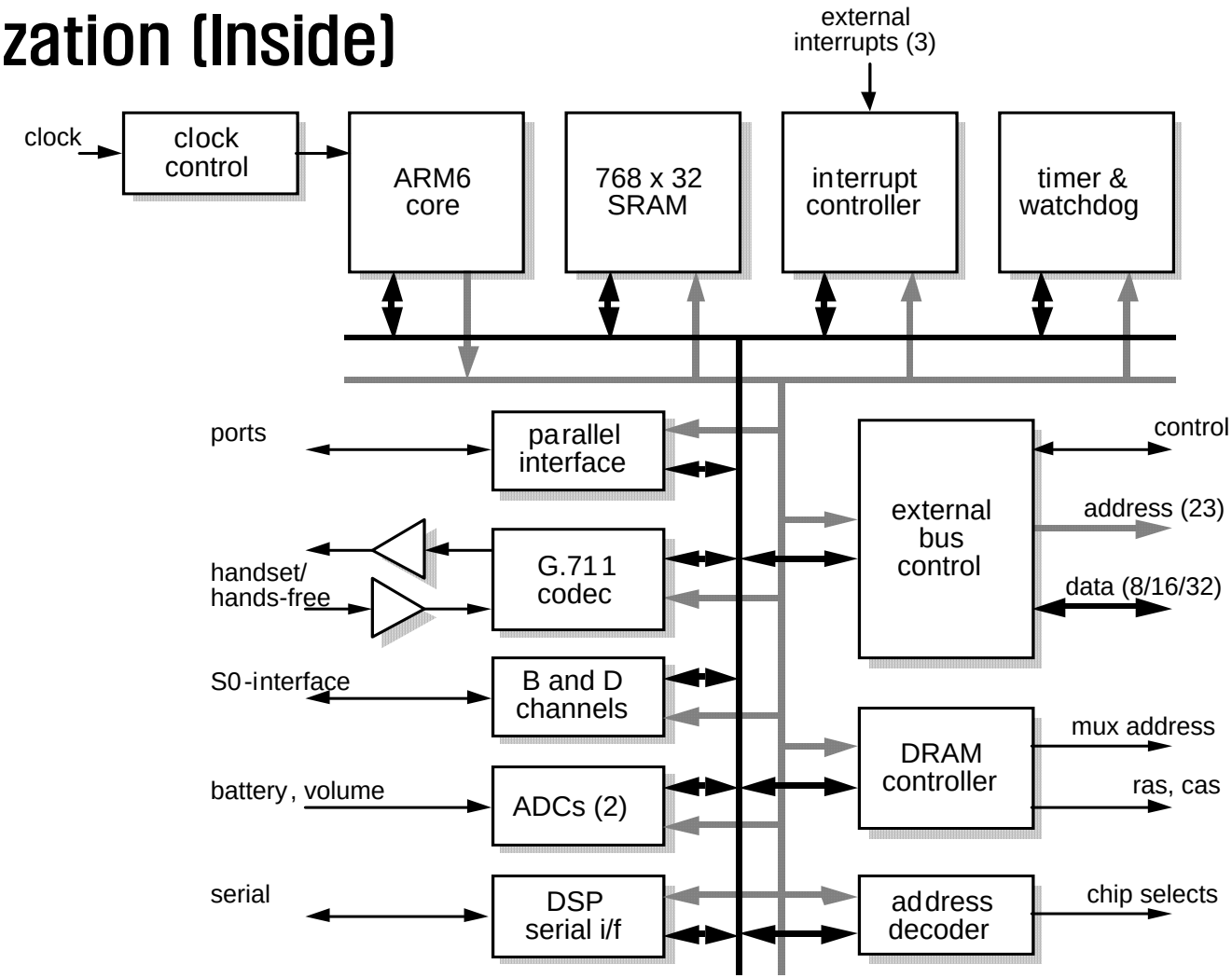
The VLSI ISDN Subscriber Processor (II)

- **Typical VIP system configuration**



The VLSI ISDN Subscriber Processor (III)

- VIP organization (Inside)



The VLSI ISDN Subscriber Processor (IV)

- Memory interface
  - Supports 8-, 16-, and 32-bit off-chip static RAMs and ROMs and 16- and 32-bit dynamic RAMs
  - Divided into 4 ranges, each with programmable number of wait states
  - 3 Kbyte on-chip RAM
- S0-interface
  - Connection to an S0-interface bus via isolating transformers and surge protection
  - PLL for data and clock recovery, framing, and low-level protocols
  - 192 Kbit/s raw data includes two 64 Kbit/s B channels (8-bit 8 KHz speech samples) and one 16 Kbit/s D channel (control purposes)
- Codec
  - G.711 codec
  - On-chip analog front end: Direct connection to a telephone handset and a hands-free microphone and speaker
  - Input and output independent programmable gains
  - Amplification stages have power-down modes to save power.

The VLSI ISDN Subscriber Processor (V)

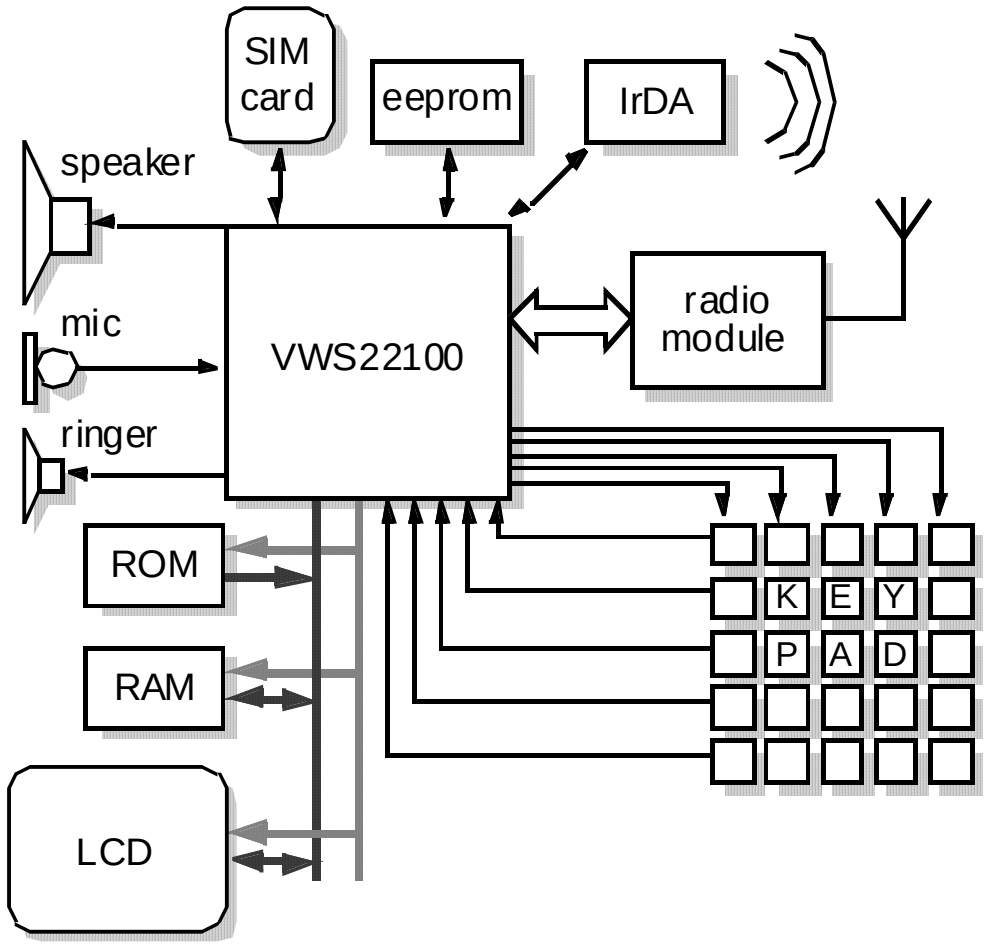
- ADCs
  - Based on timing how long it takes to discharge a capacitor to the input voltage level
  - Very simple way to measure slowly varying voltages
    - Comparator and counter
  - Measure the voltage from a volume control potentiometer or to check the battery voltage in a portable application
- Keypad interface
  - Parallel output ports to strobe the columns of the keypad
  - Parallel input ports with internal pull-down resistors to sense the rows
  - Key press will generate an interrupt:
    - ARM can activate individual columns and sense rows.
- Clocks and timers
  - 38.864 MHz and 460.8 KHz during power-down
  - Watchdog at every 1.28 sec
  - 2.5 ms timer interrupts for DRAM refresh and multitasking.

1.9 The OneC VWS22100 GSM Chip

- OneC VW22100
  - Developed by VLSI Technology, Inc
  - System-on-chip design for GSM mobile telephone handset
  - All the functions required in a handset with addition of external program and data memory and a suitable radio module
  - Example: Samsung SGH2400, a dual-band (GSM 900/1800) handset with hands-free voice-activated dialing ->

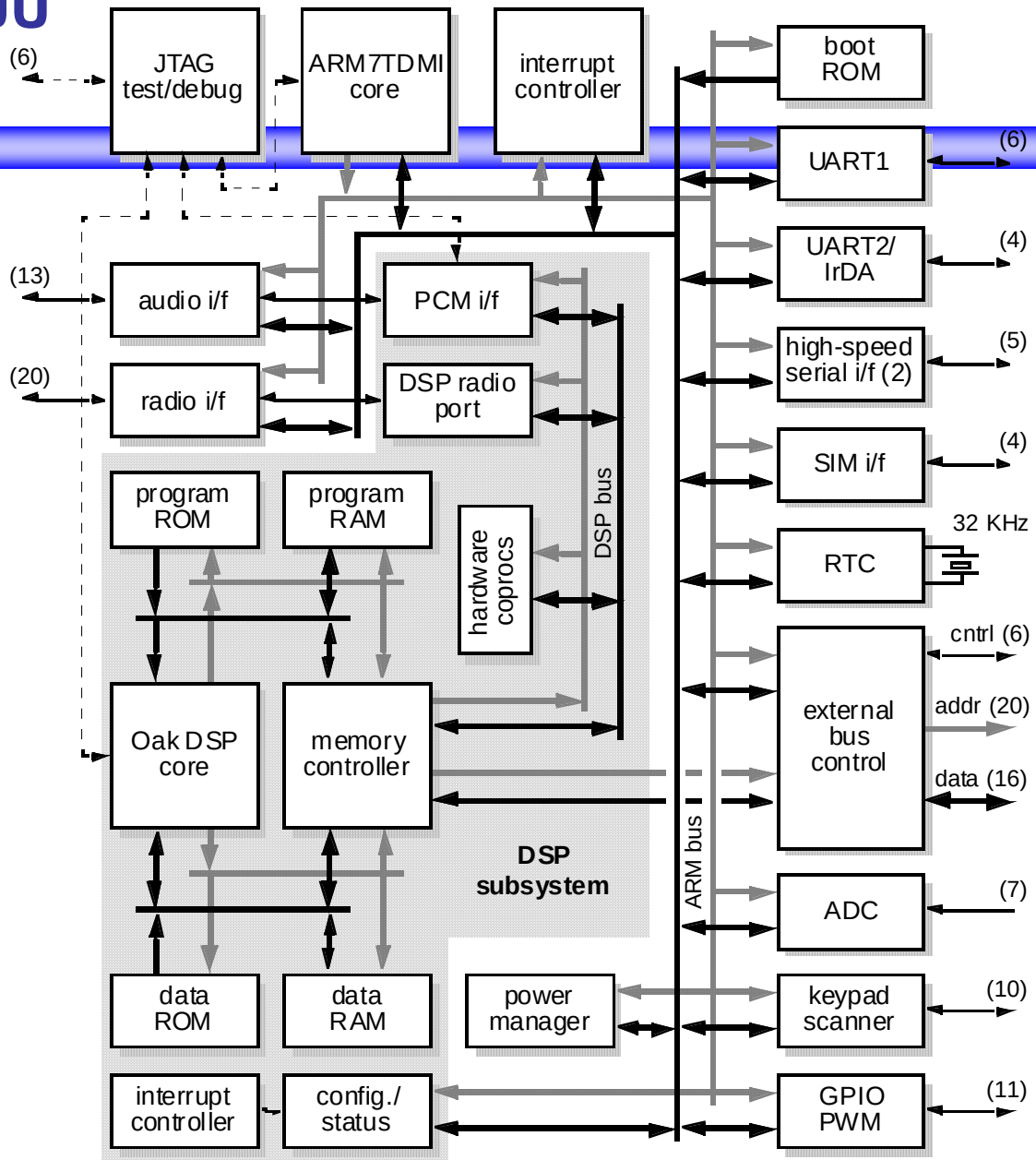
The OneC VWS22100 GSM Chip (II)

- **Typical GSM handset architecture**



The OneC VWS22100 GSM Chip (III)

- VWS22100 organization
  - ARM7TDMI core
    - General purpose controller
    - GSM protocol layers
  - DSP core
    - Baseband signal processing



The OneC VWS22100 GSM Chip (IV)

- DSP subsystem
  - Based on the 16-bit Oak DSP core
  - Real-time signal processing functions
    - Voice coding
    - Equalization
    - Channel coding
    - Echo cancellation
    - Noise suppression
    - Voice recognition
    - Data compression
- ARM7TDMI subsystem
  - Responsible for the system control functions
    - The user interface software
    - The GSM protocol stack
    - Power management
    - Driving the peripheral interface
    - Running some data applications

The OneC VWS22100 GSM Chip (V)

- On-chip debug
  - Single JTAG interface
    - ARM7TDMI EmbeddedICE module
    - Debug technology on the Oak DSP core
    - Other test and debug facilities
- Power management
  - Global and selective power-down modes
  - The ability to slow down the system clock in idle mode
  - The analog circuits also can operate at reduced power
  - The on-chip pulse-width modulation outputs control battery charging
  - The on-chip ADCs provide for the monitoring of the temperature and battery voltage to give optimum operation.

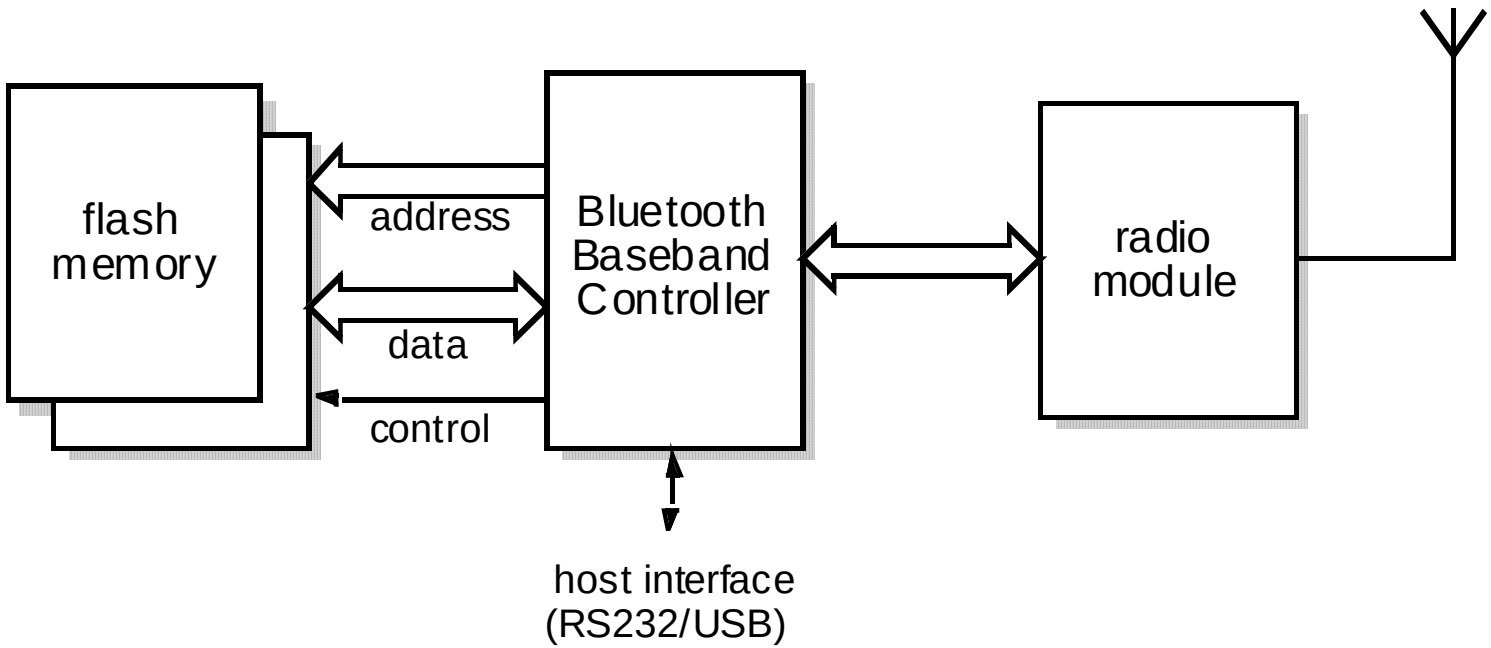
1.10 The Ericsson–VLSI Bluetooth Baseband Controller

- Bluetooth
  - De-facto standard for wireless data communication for the 2.4 GHz band
  - Consortium of Ericsson, IBM, Intel, Nokia, and Toshiba
  - Support short-range communication (to 10 m range) using radio communication with 1 Mbit/s
  - Robust communication in a noisy and uncoordinated environment
    - Frequency hopping scheme and forward error correction
  - For laptop, cellular telephone, printer, PDA, desktop, fax, keyboards, and so on
  - Provide bridge to existing networks

- Bluetooth 'piconet'
  - Bluetooth units dynamically form ad hoc 'piconets', which are groups of 2 to 8 units that operate the same frequency-hopping scheme
  - One of the units will operate as master: Defines the clock and hopping sequence.

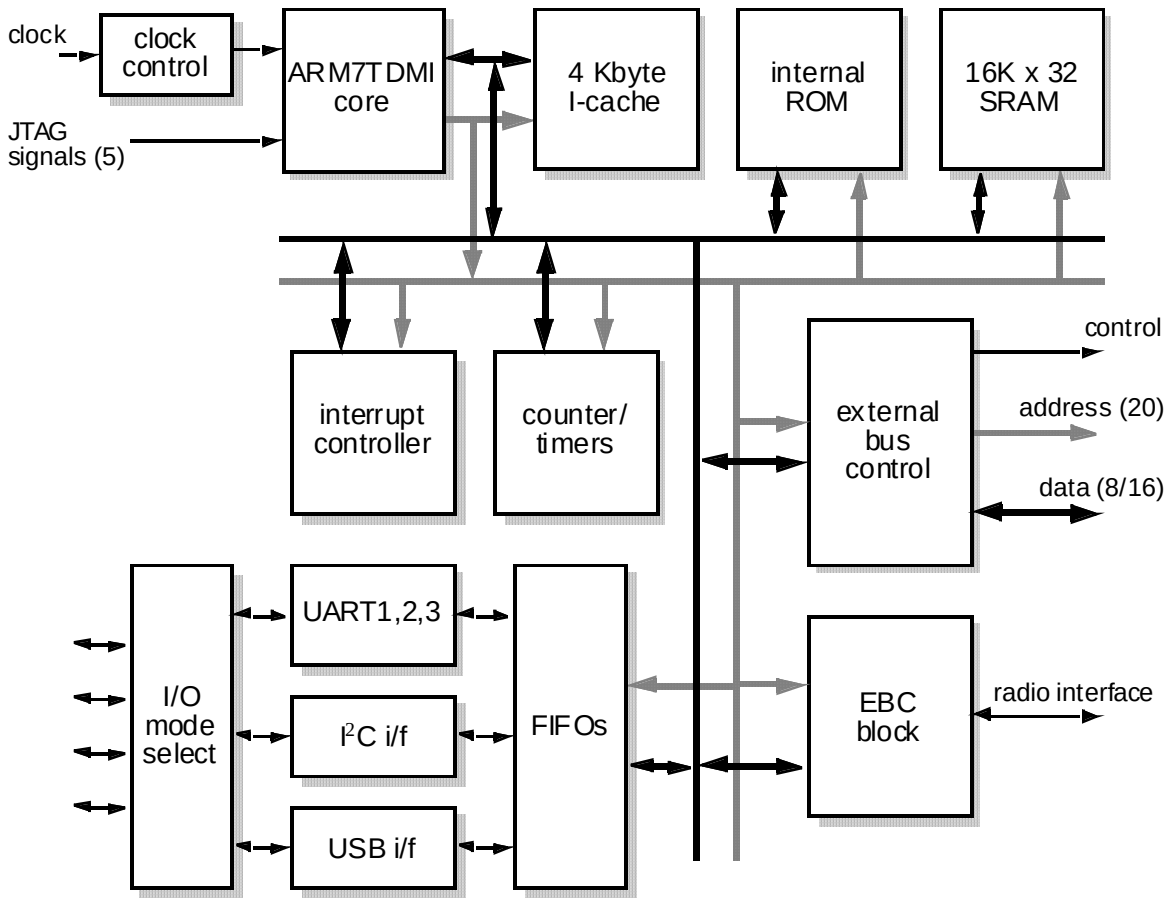
The Ericcson–VLSI Bluetooth Baseband Controller (II)

- Bluetooth system
  - A typical Bluetooth system



The Ericcson–VLSI Bluetooth Baseband Controller (III)

- Bluetooth controller organization



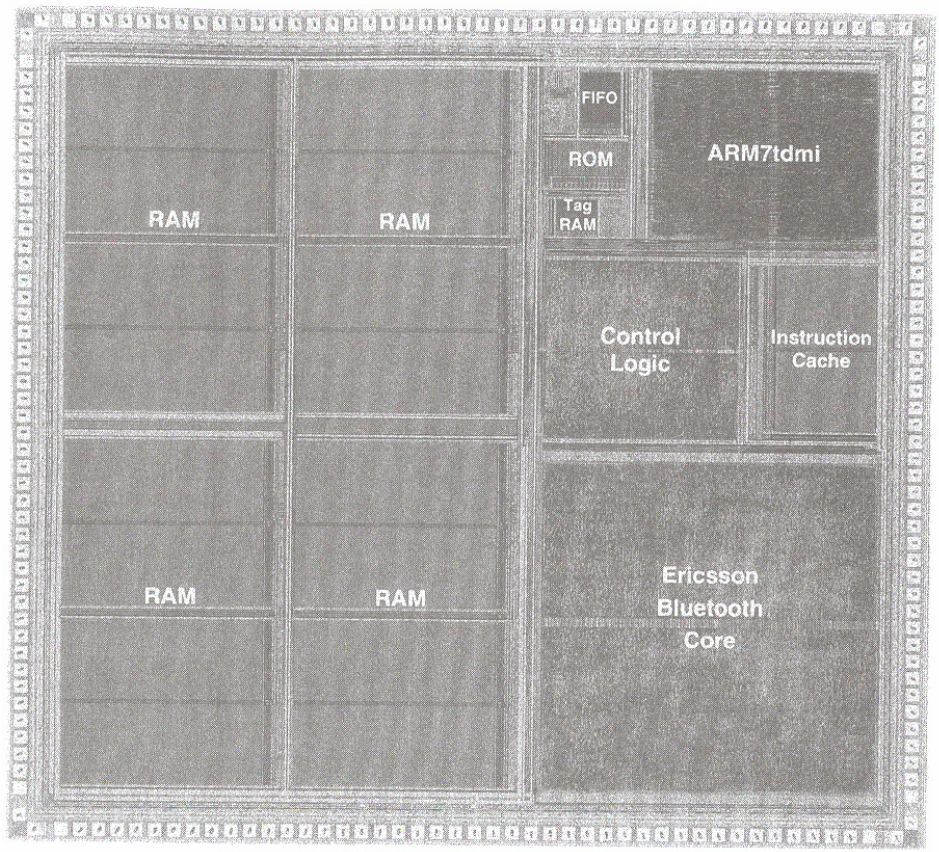
The Ericcson-VLSI Bluetooth Baseband Controller (IV)

- **Ericsson Bluetooth core**
  - Power-optimized hardware block
  - Handles all the Link Controller functionality within the Bluetooth specification
  - Interface logic to a Bluetooth radio communication
  - Performs all the packet-handling functions for point-to-point, multislot, and point-to-multipoint communications
  - Combination of circuit and packet switching

- **Power management**
  - 1. On-line: all blocks are clocked at their normal speed. The ARM7TDMI core clock 13 to 40 MHz. 40 mA max.
  - 2. Command: The ARM7TDMI clock is slowed down by the insertion of wait states
  - 3. Sleep: The ARM7TDMI click is stopped. 0.3 mA.
  - 4. Stopped: The clock oscillator is turned off.

The Ericcson–VLSI Bluetooth Baseband Controller (V)

- Bluetooth silicon
  - Photograph of a Bluetooth die –>
  - Bluetooth characteristics
    - Process 0.35 um
    - Transistors 4,300,000
    - MIPS 12
    - Metal layers 3
    - Die area 20 mm^2
    - Power 75 mW
    - Vdd 2.5 V
    - Clock 0–13 MHz
    - MIPS/W 160



1.11 The ARM7500 and ARM7500FE

- Features
  - Highly integrated single-chip computer
  - Combines the major components of the Acorn Risc PC

  - Principal macrocells
    - The ARM CPU core
    - The FPA10 floating-point coprocessor (ARM7500FE)
    - The video and sound macrocell
    - The memory and I/O controller

The ARM7500 and ARM7500FE (II)

- The ARM CPU core
  - Contains most of the functionality of the ARM710
    - ARM7TDMI without Thumb and embedded debug support
  - Reduced cache 4 Kbytes (from 8 Kbytes)
    - 4-way set-associative mixed instruction and data cache
  - Memory management unit
    - Based on a 2-level page table
    - 64-entry translation look-aside buffer
  - A write buffer

- The FPA10 floating-point unit
  - Up to 6 MFLOPS at 40 MHz

The ARM7500 and ARM7500FE (III)

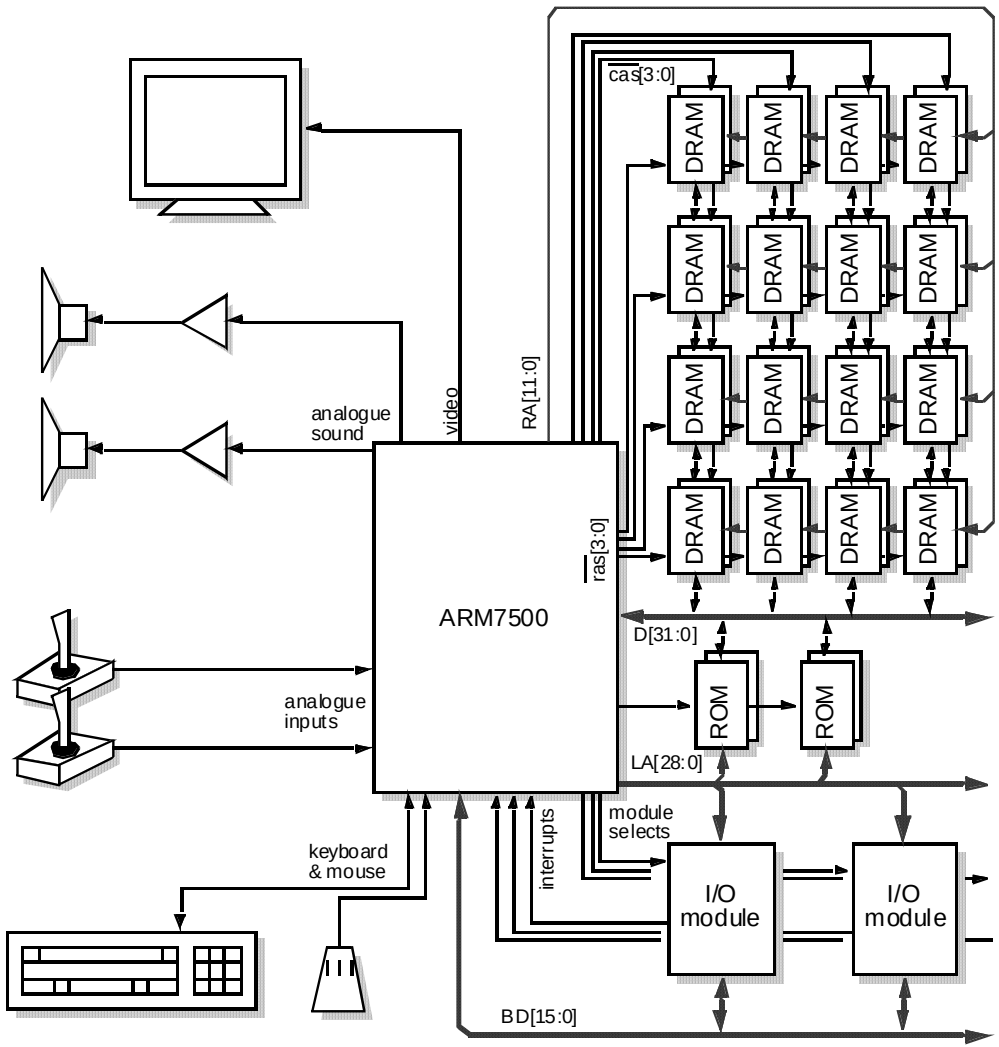
- The video and sound macrocell
  - Video controller
    - Generate displays using a pixel clock of up to 120 MHz
    - 256-entry color palette with on-chip 8-bit DACs for RGB
    - Additional control bits for external mixing and fading
    - Support a separate hardware cursor
    - Can drive a high-resolution color monitor or single- or double-panel grey-scale or color LCD
  - Sound controller
    - 8 independent channels of 8-bit analog stereo sound
    - Played through an on-chip exponential DAC
    - 16-bit sound samples through a serial digital channel and an external CD-quality DAC
  - DMA controller for video/audio data channels

The ARM7500 and ARM7500FE (IV)

- The memory and I/O controller
  - Memory controller
    - Direct connection of up to four banks of DRAM and two banks of ROM
    - Programmed to be 16 or 32 bits wide
    - Double access for 32-bit quantities in 16-bit banks
  - DRAM controller
    - Page mode accesses for sequential cycles in bursts of up to 256 transfers
    - Supports a range of DRAM refresh modes
  - ROM controller
    - Supports burst mode
  - 3 DMA controller
    - Handle data streams for video, cursor, and audio channels
  - I/O controller
    - Manages 16-bit off-chip I/O bus
    - Number of on-chip interfaces: 4 comparators, 2 serial ports, counter/timers, 8 general-purpose open-drain I/O lines, and programmable interrupt controller.

The ARM7500 and ARM7500FE (V)

- **Typical ARM7500 system diagram**

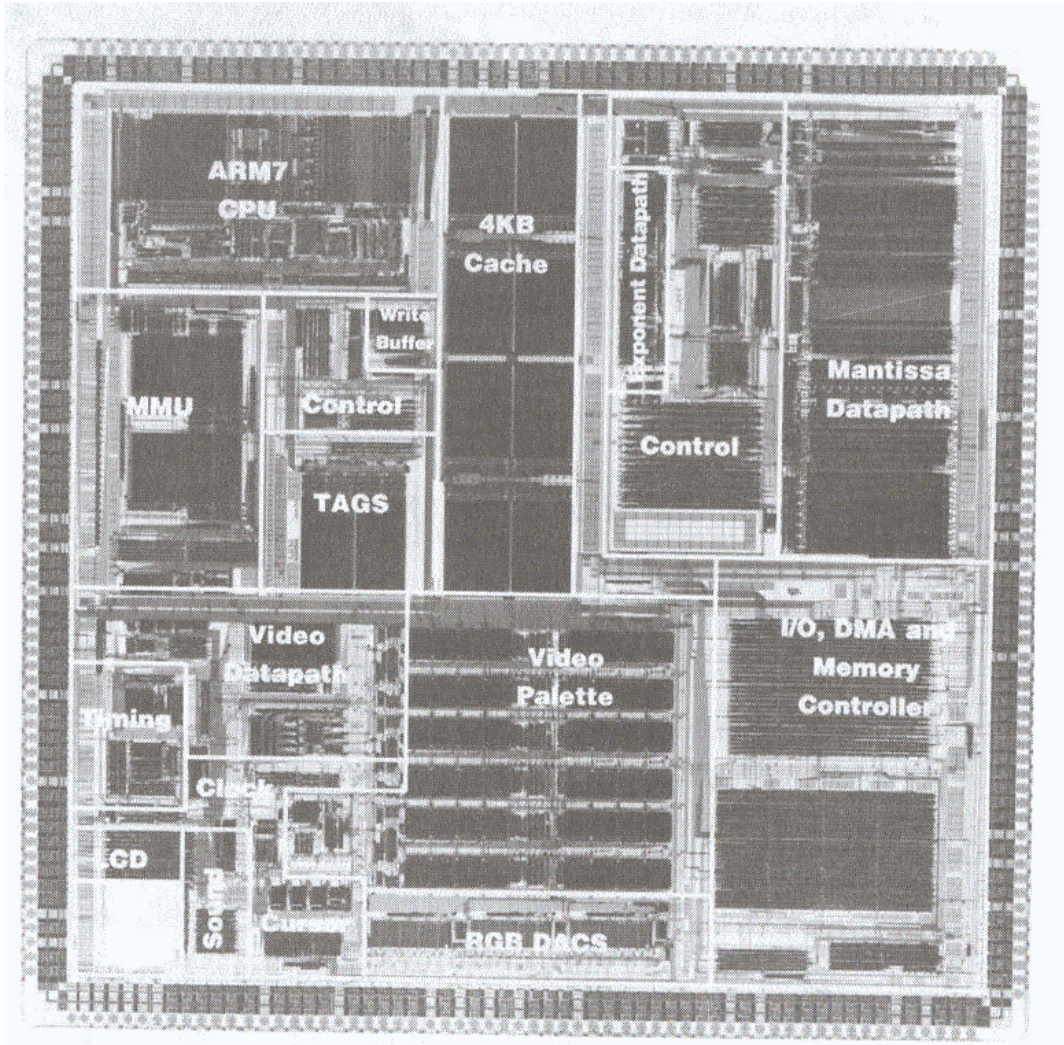


The ARM7500 and ARM7500FE (VI)

- Applications
  - Low-cost versions of the Acorn Risc PC
  - Online Media interactive video set-top box
    - Restricting the video data stream to normal DRAM
  - High-resolution displays
    - 1280 x 1024 and above the number of colors become restricted due to the bandwidth limitations of standard DRAM
  - Ideally suited
    - LCD at VGA (640 x 480)
    - TV quality display
  - Hand-held test equipment
  - Multimedia applications.

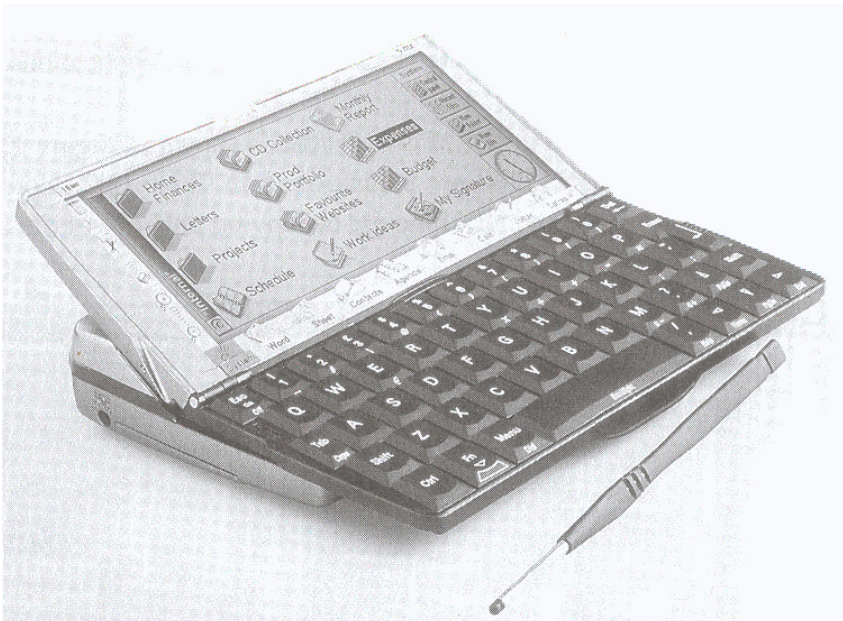
The ARM7500 and ARM7500FE (VII)

- ARM7500 silicon ->
  - 5% ARM core area
- ARM7500 characteristics
  - Process 0.6 um
  - Transistors 550,000
  - MIPS 30
  - Metal layers 2
  - Die area 70 mm^2
  - Power 690 mW
  - Vdd 5 V
  - Clock 0-33 MHz
  - MIPS/W 43



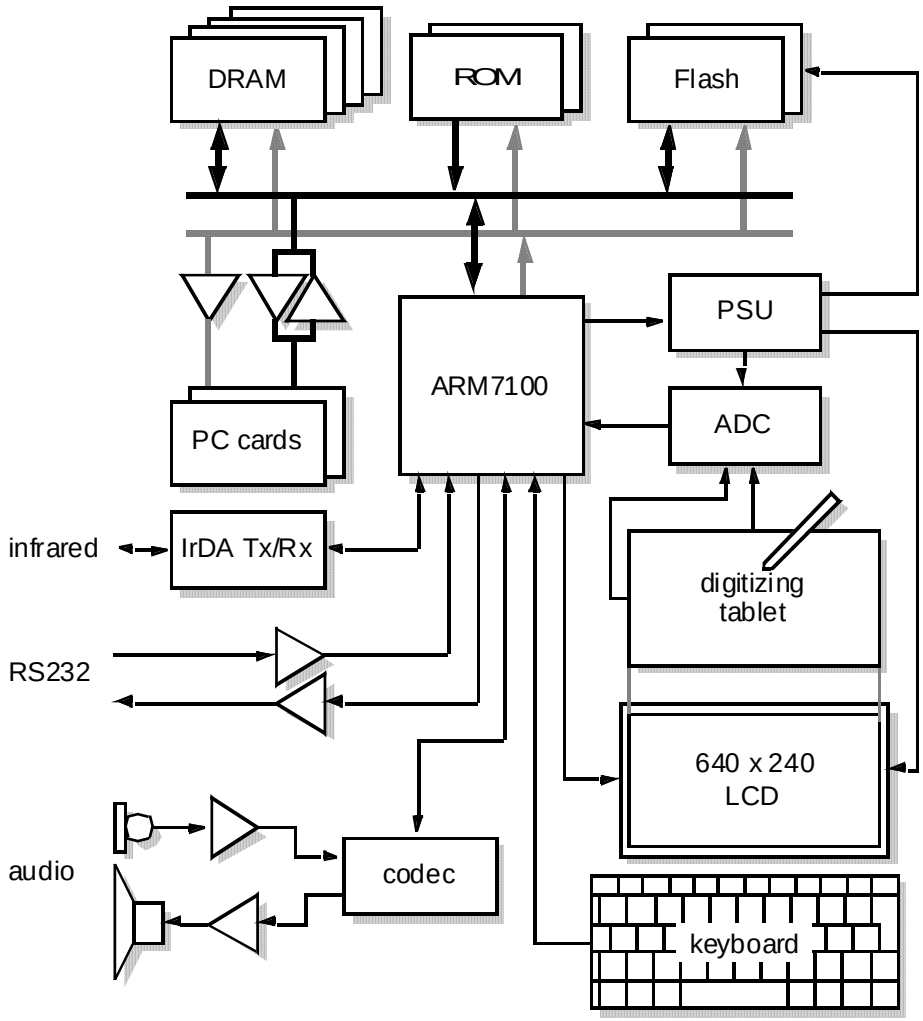
1.12 The ARM7100

- Features
  - Highly integrated microcontroller
  - Suited to a range of mobile applications
    - Smart mobile phones and palm-top computers
    - Psion Series 5MX ->



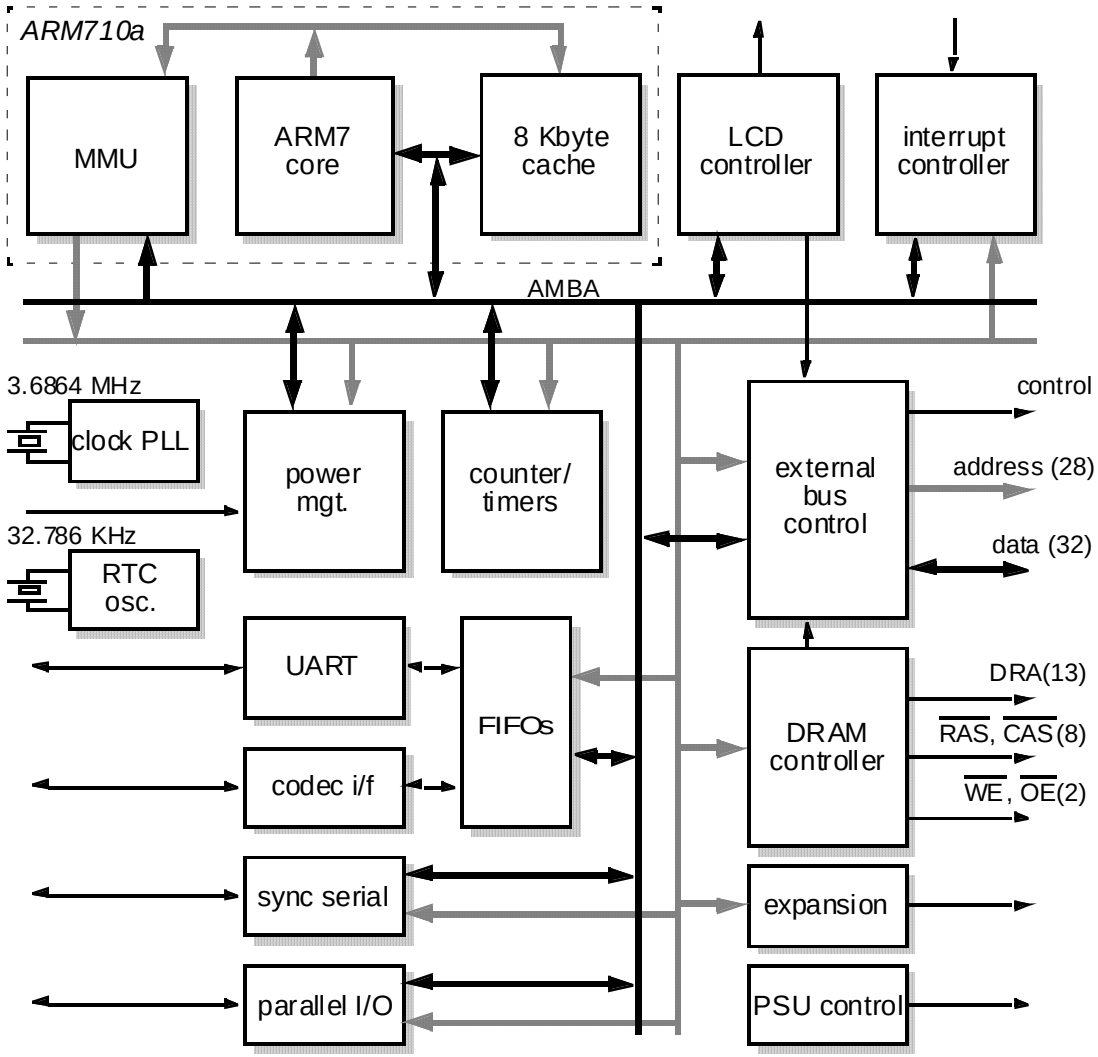
The ARM7100 (II)

- The Psion Series 5 hardware organization
  - Principal user input devices
    - Keyboard: parallel I/O
    - Stylus pointing device: transparent digitizing tablet overlaid on the LCD display
    - Infrared via ADC
  - Communication
    - RS232C serial interface
    - IrDA compliant infrared interface for wireless connection to printers, modems, and host PCs
    - Audio codec: microphone and speaker



The ARM7100 (III)

- ARM7100 organization
  - ARM710a CPU
  - ARM MMU
  - 8 Kbyte 4-way associative quad-word line cache
  - 4-address 8-data word write buffer
  - AMBA bus
  - Peripherals
    - LCD controller
    - Serial & parallel I/O ports
    - Interrupt controller
    - 32-bit external bus interface
    - DRAM controller

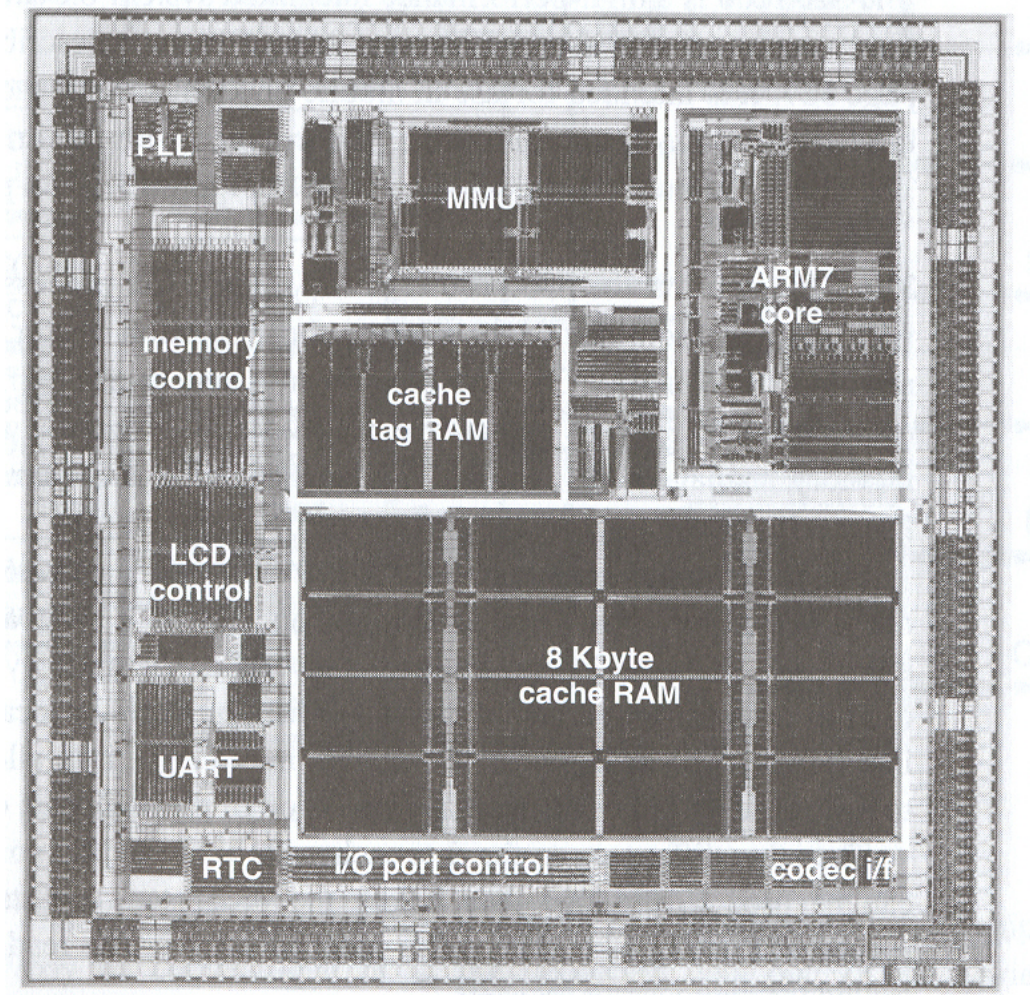


The ARM7100 (IV)

- Power management
  - Intended for use in battery-powered equipment
    - High performance in response to user input
    - Operate at very low power consumption levels
  - Levels
    - Full operation mode: 14 MIPS, 24 mA at 3 V
    - Idle mode: CPU stopped but other systems running. 33 mW
    - Standby mode: 32 KHz running. 33 uW
  - Other features to enhance power-efficiency
    - Support for self-refresh DRAM.

The ARM7100 (V)

- ARM7100 silicon →
- ARM7100 principal characteristics
  - Process 0.6 um
  - Transistor N/A MIPS 30
  - Metal layers 2
  - Die area N/A
  - Power 14 mW
  - Vdd 3.3 V
  - Clock 18.432 MHz
  - MIPS/W 212

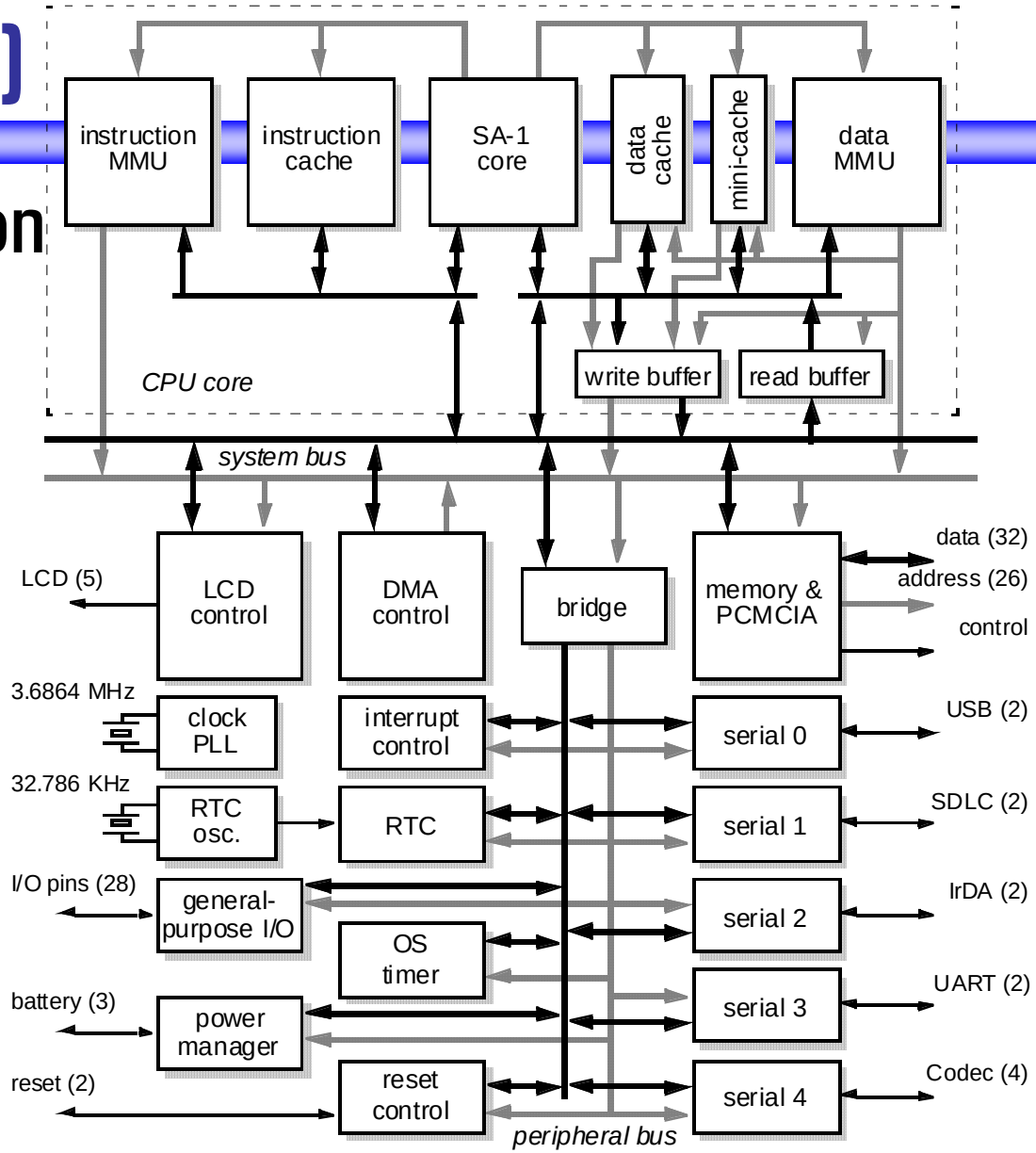


1.13 The SA-1100

- Features
  - High-performance integrated system-on-chip
  - Based on a modified version of SA-110 StrongARM CPU core
  - Intended for use in mobile phone handsets, modems, and other handheld applications
  - High performance with minimal power consumption.

The SA-1100 (II)

- SA-1100 organization



The SA-1100 (III)

- CPU core
  - SA-1 processor core
  - Exception vector relocation mechanism (for Windows CE)
  - 16 Kbyte instruction cache using a 32-way associative CAM-RAM structure with 8-word lines
  - MMU with ProcessID mechanism (for Windows CE)
  - 8 Kbyte 32-way associative data cache in parallel with a 512 byte 2-way set-associative cache
    - Allow large data structures to be cached without causing major pollution of the main data cache
  - Addition of read buffer
    - Pre-load data before the processor requests
  - Addition of hardware breakpoint and watchpoint registers.

The SA-1100 (IV)

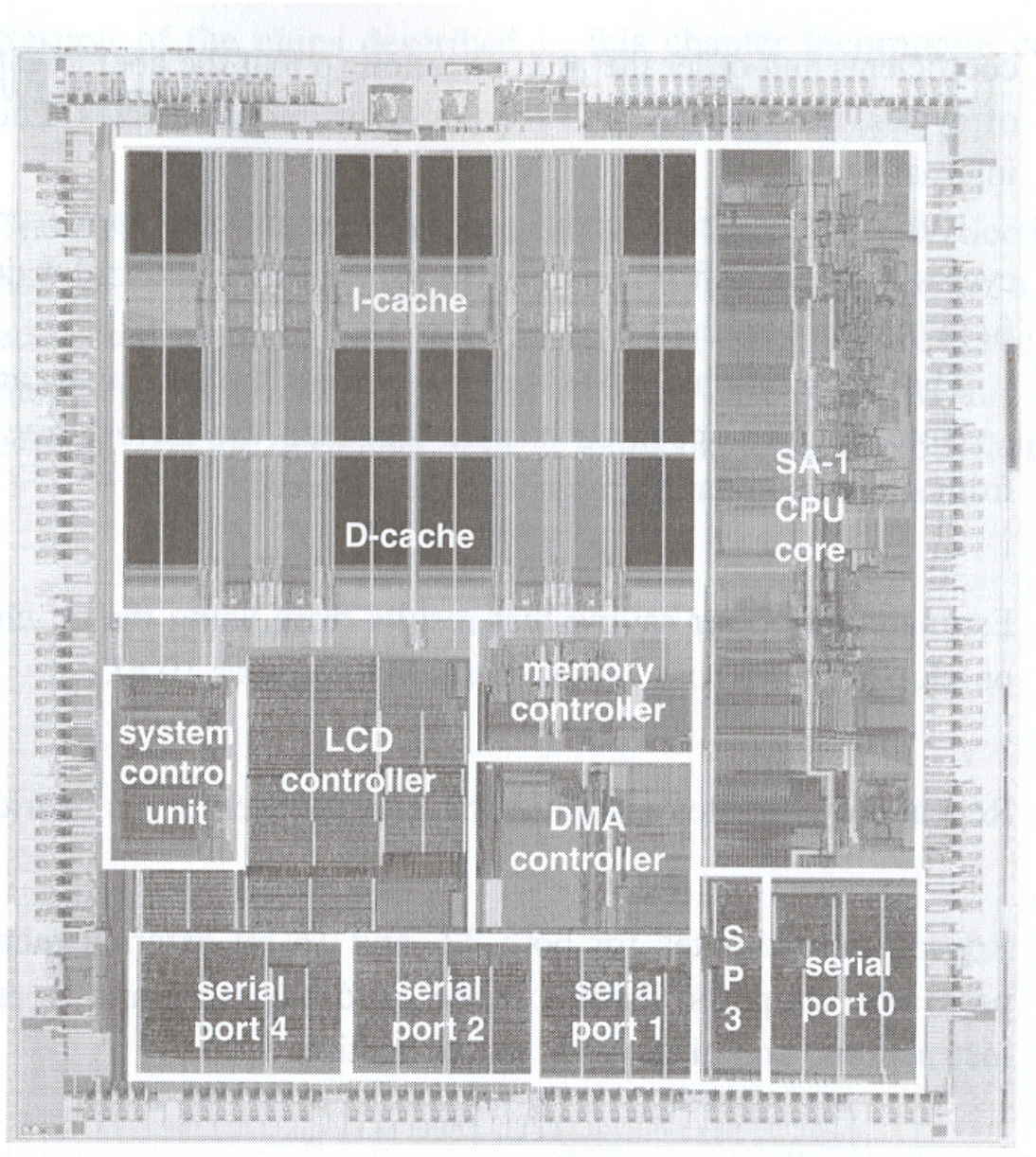
- Memory controller
  - Up to 4 banks of 32-bit off-chip DRAM
    - Conventional or 'extended data out (EDO)' variety
    - ROM, flash, and SRAM are also supported
  - PCMCIA interface
    - Two card slots are supported with some external 'glue' logic
- System control
  - On-chip
    - A reset controller
    - A power management controller that handles low-battery warnings and switches the system between its various operating modes
    - An operating system timer block that supports general timing and watchdog functions
    - An interrupt controller
    - A real-time clock that runs from a 32 KHz crystal source
    - 28 general-purpose I/O pins.

The SA-1100 (V)

- Peripherals
  - LCD controleIr
  - Serial ports: USB, SDLC, IrDA, codec, and standard UART
  - 6-channel DMA
- Bus structure
  - Two buses connected through a bridge
    - The system bus: connects all the bus masters and the off-chip memory
    - The peripheral bus: connects all the slave peripheral devices
  - Similar to AMBA ASB-APB split
    - Minimizes the bus width
    - Reduces the complexity and cost
- Applications
  - Off-chip memory: DRAM and ROM/flash
  - Necessary interface electronics for the various peripheral interfaces, display, and so on
  - Very simple at the PCB level, yet very powerful processing capability and sophisticated system architecture.

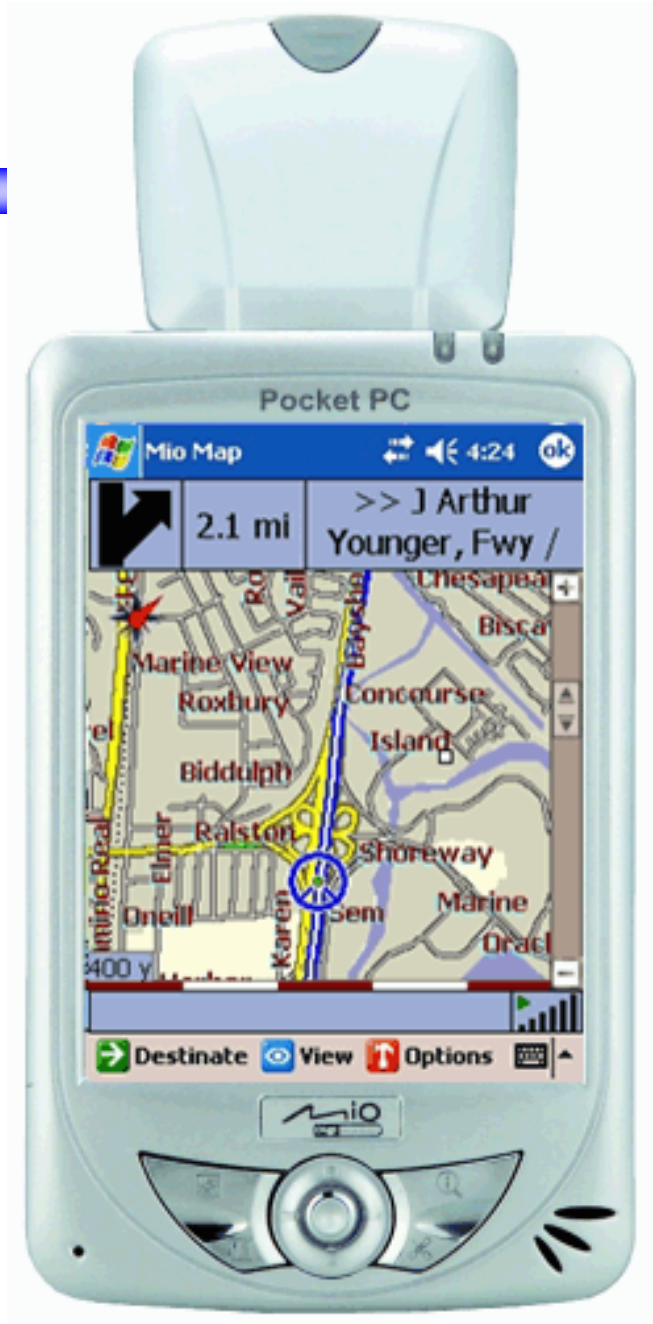
The SA-1100 (VI

- SA-1100 silicon ->
- Characteristics
  - Process 0.35 um
  - Transistors 2,500,000
  - MIPS 220/250
  - Metal layers 3
  - Die area 75 mm^2
  - Power 330/550 mW
  - Vdd 1.5/2V
  - Clock 180/220 MHz
  - MIPS/W 665/450



1.14 Mio 168

- Pocket PC with Integrated GPS
  - Runs on Windows Mobile 2003 for Pocket PC
  - Utilizes an Intel XScale processor
  - A 16-bit TFT LCD display with LED backlighting offers up to 65,536 colors
- Bundled with a complete navigation software package
  - Routing: Easy-to-follow turn-by-turn visual and voice prompts guide you to your destination
  - Plan trips and optimize routes with multi-point routing feature
  - Automatic route recalculation suggests an alternate route if you take a wrong turn.



Function		Specification
CPU		Intel® Xscale 300 MHz
Operating System		Windiws Mobile™ software for Pocket PCs
Display		3.5 color Transflective LCD, LED Backlighting, 240 x 320, 65K colors
Memory		32MB Flash ROM. 64MB SDRAM
Audio		Voice Recording(Mono). MP3 Playback support. Media Player
I/O	Input Method	Stylus pen/Software kdyboard/Handwriting Recognition
	Expansion Slot	SD/MMC. SD IO
	Microphone	Builit-in type x 1(Mono)
	Speaker	Builit-in Monaural type speaker x 1
	Headphone	2.5mm Mini jack x 1
	USB	USB 1.1 Client for ActiveSync
	Infrared	IrDA (SIR). Consumer IR (4 meters)
	battery	Embedded Lithium Ion Battery 1350mAh Active:12 hours(fully charged main battery, w/o GPS) Suspend:21 days(fully charged main battery)
Dimension		112.8 mm (H) x 69.6 mm (W) x 16.3~24.15mm (D)
Weight		147g
Power Supply		Input 100~240VAC; Output 5VDC, 1A DC